(19) Europäisches Patentamt
Europ an Pat nt Offic
Office uropé n des brevets

(11) Publication numb r : **0 613 151 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **94301320.1**

(22) Date of filing : **24.02.94**

(51) Int. Cl.[5] : **G11C 16/06**

(30) Priority : **26.02.93 JP 38112/93**
14.07.93 JP 173987/93
22.10.93 JP 264725/93

(43) Date of publication of application :
31.08.94 Bulletin 94/35

(84) Designated Contracting States :
DE FR GB

(71) Applicant : **KABUSHIKI KAISHA TOSHIBA**
72, Horikawa-Cho
Saiwai-ku
Kawasaki-shi Kanagawa-ken (JP)

(72) Inventor : **Sukegawa, Hiroshi, c/o Intellectual Property Div.**
Toshiba Corp.,
1-1-1 Shibaura,
Minato-ku
Tokyo (JP)

(74) Representative : **BATCHELLOR, KIRK & CO.**
2 Pear Tree Court
Farringdon Road
London EC1R 0DS (GB)

(54) Semiconductor memory system including a flash EEPROM.

(57) A semiconductor memory system including A flash EEPROM comprises a first flash EEPROM (101, 102, 103) included in the first memory drive, a second flash EEPROM (104, 105, 106) included in the second memory drive, and an access controller (132) for controlling access to the first and second flash EEPROMs (101-106). The access controller (132) includes an address converting means for converting a logical address from a host system into a physical address, according to an address conversion table 150 which indicates correspondence between logical addresses and physical addresses of the first and second memory drives. The access controller (132) further includes memory accessing means, coupled to each of the first and second flash EEPROMs (101-106), for accessing a selected EEPROM according to the physical address from the address converting means.

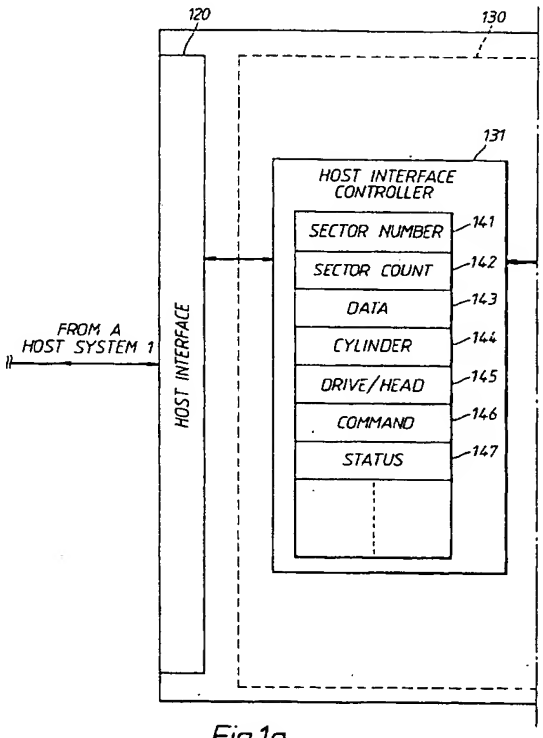


Fig.1a

EP 0 613 151 A2

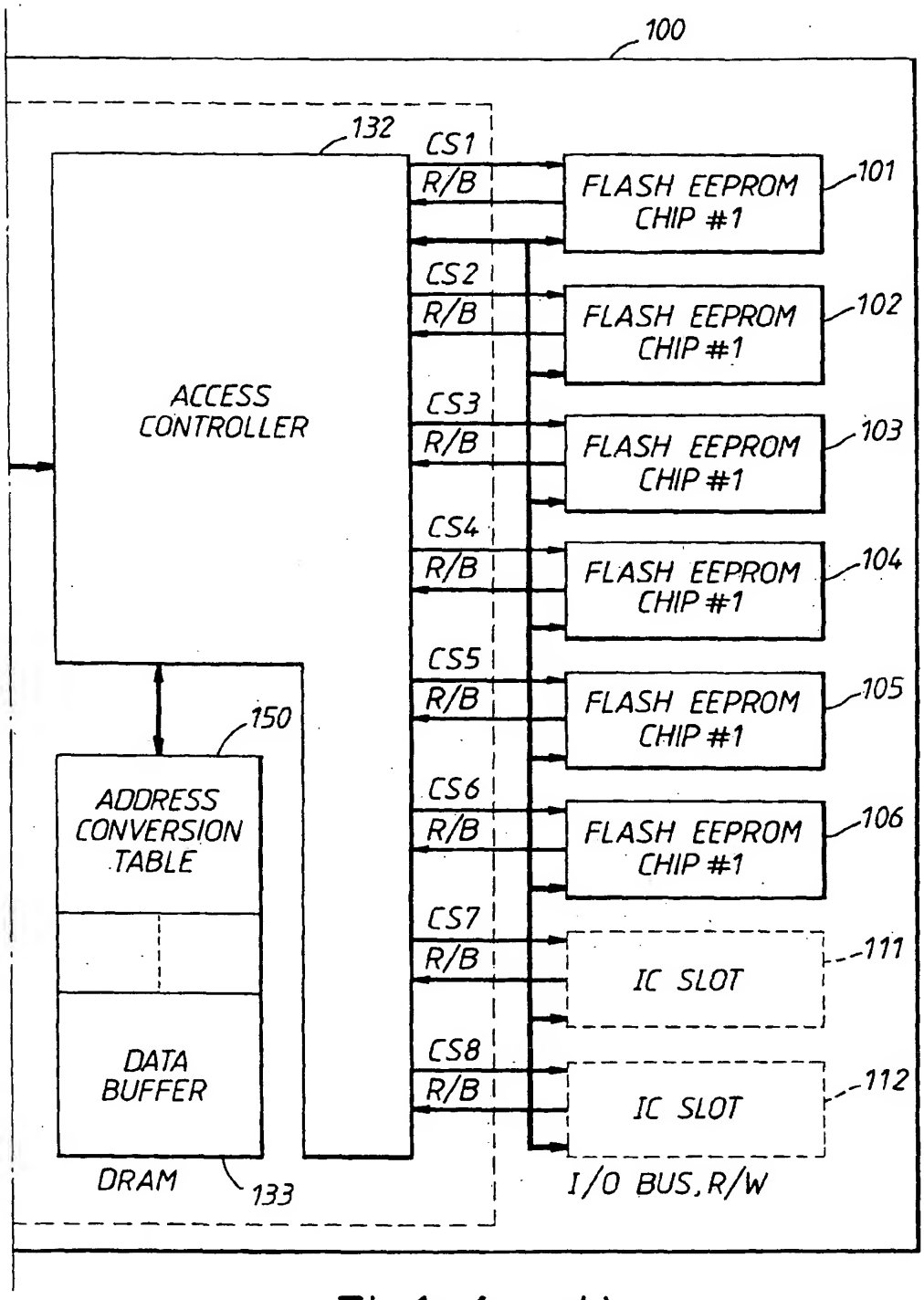


Fig.1a (cont)

The present invention relates to a semiconductor memory system equipped with a flash EEPROM (Electrically Erasable and Programmable Read Only Memory) which is a non-volatile memory that is electrically and collectively erasable and rewritable.

More particularly, this invention relates to a semiconductor memory system that can realize miniaturization.

Most of conventional information processing systems, such as a work station and a personal computer, use a magnetic disk drive as a secondary memory device. The magnetic disk drive has advantages such as a high recording reliability and low bit price while having some shortcomings such as its being large and susceptible to physical impact.

The operational principle of magnetic disk drives is to move a magnetic head on a rotating disk to write or read data on or from that disk. The mechanical moving portions, such as the rotatable disk and the magnetic head, may malfunction or may be damaged when a physical shock is applied to the disk drive. Further, the necessity of those mechanical movable portions impedes making the whole drive more compact.

Accordingly, these deficiencies represent a significant problem when loading the magnetic disk drive into a small portable computer, such as a note book type or pen type personal computer.

Today, therefore, there is a need for a semiconductor memory system which is small in size and not susceptible to physical impact. The semiconductor memory system usually has a plurality of EEPROM chips. The semiconductor memory system can be used as a secondary memory device instead of a magnetic disk drive. A computer system can use the semiconductor memory system by a same method of access for the magnetic disk drive.

The semiconductor memory system has several merits in the case of use in a personal computer.

As one merit, a size of the semiconductor memory system can be smaller than a size of the magnetic disk drive. However, a EEPROM chip used in the semiconductor memory system is very expensive. Therefore, there is a need for a product and parts cost of a semiconductor memory system that is as low as possible.

As another merit, the semiconductor memory system is readily adapted to control EEPROM and is resistant to breakage because it does not include movable parts. However, a cell array of an EEPROM is deteriorated by rewrite operations (erase and write) little by little. In time, one of the flash EEPROMs in the semiconductor memory system will have some memory blocks which cannot be rewritten by the semiconductor memory system, because dispersion of r - write times varies widely. Therefore the semiconductor memory system will be r quired to be able to exchange a unit of an EEPROM chip, when the semiconductor memory system is used as the secondary memory device in a computer, such as a portable type of computer.

It is an object of the present invention to provide a semiconductor memory system which can achieve minimization and low cost by reducing the number of component parts.

In accordance with the present invention there is provided a peripheral semiconductor memory system including first and second memory drives. The system comprises a first flash EEPROM included in the first memory drive, a second flash EEPROM included in the second memory drive, and means for controlling access to the first and second flash EEPROMs. The access controlling means includes an address converting means for converting a logical address from a host system into a physical address, according to first and second file management information which indicates correspondence between logical addresses and physical addresses of the first and second memory drives, respectively. The access controlling means further includes memory accessing means, coupled to each of the first and second flash EEPROMs, for accessing a selected EEPROM according to the physical address from the address converting means.

Brief description of the drawings

The present invention will be apparent from the following description, in connection with the following figures, of which:

Fig.1a is a block diagram showing an embodiment of a semiconductor memory system according to the present invention.

Fig.1b shows an address conversion table, which is referred by an access controller in the semiconductor memory system as shown in Fig.1a for converting logical address into physical address.

Fig.1c shows a memory block information table stored in a flash EEPROM chip,

Fig.2 shows a conceptual diagram of a semiconductor memory system which is controlled as two drives by a host system.

Fig.3 shows a physical arrangement of a part of the embodiment shown in Fig.1

Fig.4 shows a type of address conversion table used in the embodiment shown in Fig.1

Fig.5 is a flow chart showing access control processing when the semiconductor memory system uses the address conversion table of the Fig.4.

Fig. 6 is a flow chart showing a process of exchanging a flash EEPROM chip for another flash EEPROM chip of the same memory capacity.

Fig. 7 is a flow chart showing a processing of exchanging a flash EEPROM chip for another flash EEPROM chip of double memory capacity.

Fig. 8 is a flow chart showing a process of expanding a flash EEPROM chip without exchanging

flash EEPROM chips.

Fig.9 is a block diagram of a single package LSI showing another embodiment of the present invention.

Fig.10 is a block diagram of the semiconductor memory system using the single package LSI shown in fig.9.

Fig 11 is an address conversion table for an access controller shown in Fig.9

Fig.12 shows a conceptual diagram of a semiconductor memory system which is controlled as two drives by a host system and which uses the single package LSI shown in Fig.9.

Fig.13 shows a physical arrangement of a host system including a semiconductor memory system structured on a memory board.

Fig.14 is a block diagram of the host system shown in Fig.13.

Fig.15 shows a physical arrangement of a host system including chips of the semiconductor memory system mounted on a mother board of the host system.

Fig.16 is a block diagram of the host and semiconductor memory systems shown in Fig.15.

Fig.17 shows a physical arrangement of a host system including connectors for inserting the single package LSI chip and a plurality of flash EEPROM chips of the semiconductor memory system, on a mother board in the host system.

Fig.18 is a block diagram of the host system having lines for determining whether or not the single package LSI chip shown in Fig.17 is inserted into its connector.

An embodiment of the present invention will be described with reference to the accompanying drawings.

Fig.1a shows a block diagram of a semiconductor memory system according to an embodiment of the present invention.

A semiconductor memory system 100, connected to a personal computer (host system 1), comprises a plurality of flash EEPROM chips 101-106, two IC slots 111 and 112, a host interface 120 and a controller unit 130, and is used as a secondary memory device for the host system in place of a hard disk drive or a floppy disk drive or a memory card, and has a PCMCIA (Personal Computer Memory Card International Association) interface or an IDE (Integrated Drive Electronics) interface, for example.

Each of the flash EEPROM chips 101-106 comprises a cell array and a plurality of peripheral logic functions, such as a row address decoder, for the cell array. Each EEPROM chip 101-106 has an input/output (I/O) register, for xample structured for 256 byt s. In ach flash EEPROM chip 101-106, a minimum unit of data amount handled in a writ or an erase operation is determined and th unit amount of data is handled together. For xample, it is assumed that the flash EEPROM allows data write operations in pag s of 256 bytes and data erase op rations in blocks of 4K bytes. In this case, for ach of the flash EEPROM chips 101-106, it is preferable to use a Toshiba 16 M-bit NAND flash EEPROM. The flash EEPROM be accessed by providing an initial memory address of an unit of data.

Each of the IC slots 111 and 112 is an expansion slot for expanding a flash EEPROM chip.

The flash EEPROM chips 101-106 and the IC slots 111 and 112 are connected to the controller unit 130 via a common I/O bus and a common read/write control line (R/W). Further, each flash EEPROM chip 101-106 and each IC slot 111 and 112 independently is connected to the controller unit 130 via a chip select signal (each CS 1-8) line and a ready/busy signal (R/B) line.

The host interface 120, like a hard disk drive connectable to a host system, has, for example, a 40-pin arrangement conforming with the IDE interface, or like an IC card installable in an IC card slot, has, for example, a 68-pin arrangement conforming with the PCMCIA interface.

The controller unit 130 comprises a host interface controller 131, an access controller 132 and a DRAM 133.

The host interface controller 131 controls communication between the host interface 120 and the access controller 132, and has several registers, including a sector number register 141, sector count register 142, data register 143, cylinder register 144, drive/head register 145, command register 146 and status register 147. These registers 141-147 are able to be read and be written by the host system 1. The sector number register 141 stores an access head sector number transmitted from the host system 1. The sector count register 142 stores a number of sectors which indicates a sector size of write or read data. The data register 143 stores write data from the host system 1 or read data to the host system 1. The cylinder register 144 stores an access cylinder number transmitted from the host system 1. The drive/head register 145 stores an access drive number and an access head number transmitted from the host system 1. The command register 146 stores a command, such as read or write, transmitted from the host system 1. The status register 147 stores status of the semiconductor memory system 100.

The DRAM 133 has a management area for storing an address conversion table 150, and so on, and a data buffer area for storing write data or read data temporarily.

Fig.1b shows the address conversion table 150.

When the host system is powered on, the access controller 132 reads memory block information table 191-196 (MBIT, as shown in Fig.1c) which is stor d in each EPROM chips 101-106, respectively. The ac c ss controll r 132 generates an address conversion

table 150 in according to the memory block information tables and each chip numbers corr sponding to each memory block information tables. The generated address conversion table 150 is stored in DRAM 133.

The address conversion table 150, which defines address conversion information for indicating a correspondence between logical addresses from the host system 1 and physical addresses of the flash EEPROM chips 101-106. Herein, the logical address, output from the host system, comprises a cylinder number, a head number, a sector number and a drive number. The physical address comprises a chip number of an EEPROM chip and an initial memory address of a sector block in the EEPROM chip.

The address conversion table 150 defines an assigned drive number 0 to the EEPROM chips number 1-3, i,e., chips 101-103 and an assigned drive number 1 to the EEPROM chip number 4-6, i,e., chips 104-106. The host system 1 uses drive number 0 for a master drive, and uses drive number 1 for a slave drive, for example.

The access controller 132 has a microprocessor and firm ware for controlling the processor, and provides access control of the flash EEPROM chips 101-106 for the host interface 120 and the host interface controller 131, in response to a disk access request supplied from the host system 1. That is, the access controller 132 reads commands and parameters stored in the registers in the interface controller 131, and controls flash EEPROM chips 101-106 in response to the contents of the registers.

The access controller 132 has a function for converting a logical address from the host system 1 into physical address of the flash EEPROM chips 101-106, according to the address conversion table 150 stored in the DRAM 133.

In the result of the address conversion table 150, the access controller 132 selects one of these flash EEPROM chip (by providing a signal to one of the chip select signal lines CS1-CS6) and generates a real memory address. The access controller 132 repeats to generate logical address still times of the value in the sector count register and sequentially provides logical addresses to the flash EEPROM chips 101-106, according to the table 150.

The access controller 132 manages rewrite (or erasing) times of each erasable block in each flash EEPROM chip 101-106 by using rewrite count information in each flash EEPROM chips 101-106. Here, a management unit of rewrite count information is an erasable block of the flash EEPROM chip, for example 4K bytes. The access controller 132 further manages attribut information, such as the number of the conn cted chips and a total memory capacity of the flash EEPROMs, by using a configuration table stored in one or more flash EEPROM chips.

The operation of the semiconductor 100 memory system will be described as follows.

The host system 1 provides command,sector size and logical addr ss (same HDD address) to the semiconductor memory system 100, if the semiconductor memory system 100 is not of active state. The host system 1 judges whether the semiconductor memory system 100 is active or non-active, by the content of the status register 147.

The host interface controller 131 in the semiconductor memory system 100 receives the command, sector size and the logical address, and stores this information in the registers 141-146.

The access controller 132 reads the contents of the registers 141-146 in the host interface controller 131, when the host system 1 provides an access request to the semiconductor memory system 100. The access controller 132 determines a physical address from the logical address structured by data in the registers 141,144,145, by referring to the address conversion table 150. The access controller 132 further generates a next logical address by incrementing by '1' the value in the register 141, and determining the next physical address from the next logical address by referring to the address conversion table 150. The access controller 132 sequentially decides physical address, according to repeating the operation still times of the value in the register 142.

The access of flash EEPROM can be achieved by a command method where an operation mode of the flash EEPROM is specified by a command.

According to a command method, first, the access controller 132 provided a chip enable (CE) signal for indicating an active state of a selected flash EEPROM chip by the address conversion table 150. Next, the access controller 132 provides a memory command for indicating an operation mode(write, read, erase, verify and so on) to the flash EEPROM chips 101-106 via a read/write control line. Next, the access controller 132 provides a memory address for indicating an access start address to flash EEPROM chip 101-106 via the I/O bus. After providing the memory address, if the operation mode is the write mode, then the access controller 132 transfers write data via the I/O bus, and if the operation mode is the read mode, then the access controller 132 receives read data from the selected flash EEPROM via the I/O bus. Here, if the operation mode is the write mode, then the access controller 132 is free from access control for the selected flash EEPROM after transferring write data to the I/O register(for example, 256 byte) in the selected flash EEPROM, and the write operation is run automatically in the selected flash EEPROM only.

The host system 1 identifies a first memory block (the flash EEPROM 101-103) with drive number 0, and identifies a second m mory block (the flash EEPROM 104-106) with drive number 1. That is, the host syst m 1 r cognizes the semiconductor memory sys-

tem 100 as having two different secondary memories. The controller unit 130 manages each of the two memory blocks independently. This concept is shown in Fig. 2.

As shown in Fig. 2, the semiconductor memory system 100 is handled as two drives, by a File Allocation Table (FAT) file system installed in the host system 1. A first memory block 181 is managed by a FAT1 stored in the flash EEPROM 101 and a second memory block 182 is managed by a fate stored in the flash EEPROM 104. Accordingly, the semiconductor memory system 100 does not write one file to the first memory block 181 and the second memory block 182 separately. That is, for example, the files of the second memory block 182 are not influenced, even if the first memory block 181 is changed or expanded.

Accordingly, a user can easily exchange the memory capacity of the first memory block 181 without influencing the files in the second memory block 182. Moreover, each of the first and the second memory block 181, 182 can have total address conversion information for address conversion table 150 without separating address conversion information with respect to association with each of memory block 181,182. In this case, address conversion table 150 generated in the access controller 132 can be selected by the host system 1.

Fig.3 shows a physical arrangement of the semiconductor memory system 100 according to an embodiment of the present invention.

Fig.3 shows only the flash EEPROMs 101-103 of the first memory block 181, typically.

The controller unit 130 and IC slots 201-203 are directly are mounted on a printed circuit board 210, but the flash EEPROM chips 101-103 are mounted on the printed circuit board 210 via IC slots 201-203. As a result, each flash EEPROM chip, the including chips 101-103 can easily be connected and disconnected by user.

Fig. 4 shows another address conversion table 250 which can be used in the access controller 132.

The address conversion table 250 does not list the drive number, but the flash EEPROM chips 101-103 and the flash EEPROM chips 104-106 have continuously assigned sector numbers. For managing the sector numbers by each drive, each value of the start sector number assigned to each of the first memory block and the second memory block must begin with 0. However, in this case, each value of the sector numbers of the second memory block 182 listed in the address conversion table 250 adds the value 0-m of real sector numbers to an offset value (n+1). As a result, the access controller 132 operates normally.

With r ference to th flow chart of Fig. 5, operations of the semiconductor memory system 100 using address conversion table 250 of Fig.4 will be described.

First, th host system 1 writes a command, such as read or write, in the command register 146 (step 11). Next, the host interface controller 131 sets a busy flag in the status register 147 (step 12). The access controller 132 determines that a command is written in the command register 146, and reads the command in the command register 146 (step 13,14). The access controller 132 evaluates the command (step 15). The access controller 132 generates a sector address for referring to the address conversion table 250, on the basis of the drive number and the sector number from the host system 1. If the drive number is 1, then the sector address is the sector number plus offset value (n+1), else the sector address is the sector number (step 16). The access controller 132 generates a physical address from logical address (having the sector address) on the basis of the address conversion table 250 (step 17). Next, the access controller 132 controls the access of one of the flash EEPROM 101-106, according to a physical address generated by the address conversion table 250 and the command (step 18). Last, the host interface controller 131 resets busy flag in the status register 147 (step 19).

In this embodiment, the host system 1 can recognize the first and second memory blocks 181,182 as independent disk drives. The FAT file system in the host system 1 independently can manage data written in the first memory block 181 and data written in the second memory block 182.

For example, even though a user replaces at least one of the EEPROM chip 104-106 of the second memory block 182 with another EEPROM chip, the files stored in the fist memory block are not influenced, because the semiconductor memory system does not write separately the first memory block and the second memory block.

Accordingly, each memory block 181,182 managed by each drive can easily be able to change capacity of the memory block, such as structuring first memory block 181 to consist of the two EEPROM chip 101,102 only, without influencing the other memory block.

More over, each memory block 181,182 managed by each drive can easily be able to replace at least one of the EEPROM chips in either memory block with another EEPROM chip without influencing the other memory block.

Next is described a memory management operation when a new flash EEPROM chip is connected to an IC slot 111.

Fig. 6 shows a process flow chart for exchanging a flash EEPROM chip, such as a flash EEPROM having an erasable block which has been rewritten more than a desired number of times, with a new flash EEPROM chip of the same size which is connected to the empty slot.

The access controll r 132 monitors and controls the number of rewrit (or erasing) times of each eras-

able block in each flash EEPROM chip 101-106 by using rewrite count information in each flash EEPROM chip 101-106. When one of the flash EEPROM chips 101-106 has an erasable block which has been rewritten more than a desired number of times, the access controller 132 provides a chip number of the particular EEPROM chip to the host system 1.

The host system 1 displays a message indicating the chip number of the chip which must be exchanged. The user connects a new flash EEPROM chip of the same size into an empty slot, such as the IC slot 111 (step 21). Next, the user inputs a command for running a utility program for enabling the use of the new flash EEPROM chip, and inputs the chip number of the exchanged chip (step 22). Here, the host system 1 provides a command for running the utility program and the chip number to the access controller 132, and the utility program is run by the MPU in the access controller 132. The access controller 132 directly copies all information stored in the exchanged chip (for example, flash EEPROM 101), into the new chip connected to the slot 111 newly (step 23). The number of the IC slot to which the new flash EEPROM chip is connected can be determined by referring to each Ready/Busy signal. For example, when the new flash EEPROM is connected to the IC slot 111, the Ready/Busy signal, indicating a state of high impedance level or ground level, changes the Ready state because of insertion of the new flash EEPROM chip. Thus, the access controller 132 can determine the number of the slot to which the new flash EEPROM is connected by change of the each Ready/Busy signal. Next, the MPU rewrites the rewrite count information in the new flash EEPROM to initialize a value '0', because the controller has copied the rewrite count information of the exchanged flash EEPROM chip into the new flash EEPROM chip, in the previous copy operation (step 24). Next, the MPU writes the address conversion table 150, to correct the chip number registered physical address to the chip number of the new flash EEPROM chip (step 25). For example, when the number of the new chip connected to the slot 111 is 7, the address conversion table 150 of Fig. 1 is connected to change the registered chip number '1' into the chip number '7'. In response to the MPU signaling an end of the exchanging operation to the host system, the host system 1 displays a message indicating an end of the exchanging operation (step 26). The user removes the exchanged flash EEPROM chip, after receiving the message from the host system (step S27).

The host system 1 can handle the new EEPROM chip as the drive 0 in the semiconductor memory system 100. Also, the memory capacity of the new flash EEPROM chip can be different from the memory capacity of the exchanged flash EEPROM chip.

Fig. 7 shows a process flow chart for exchanging a flash EEPROM chip (chip type 1), such as a flash EEPROM chip having erasable block which has been rewritten more than a desirable number of times, for a new flash EEPROM chip of double memory capacity(chip type 2) connected to an empty slot.

The user connects a new flash EEPROM of the chip type 2 to the empty slot, such as the slot 111 (step 31). Next, the user inputs a command for running a utility program for enabling the use of the new flash EEPROM chip, and inputs the chip number of the exchanged chip (step 32). Here, the host system 1 provides a command for running the utility program and the chip number to the access controller 132, and the utility program is run by the MPU in the access controller 132.

The access controller 14 recognizes a chip type of the new flash EEPROM chip inserted into the slot 111. A recognizing method for the chip type can be achieved by whether or not the access controller 132 reads an ID stored at a head address (B0B0) of a second chip area of the flash EEPROM. The second chip area is an area in excess of the memory size of the chip being replaced. For example, when an exchanged chip has 4 M byte and a new chip has 8 M byte, a second chip area is the area of the new chip in excess of 4 M byte. If the new flash EEPROM chip does not have a second chip area, then the address B0B0 does not exist. Thus, the access controller 132 determines the chip type (step 33,34). In this case, if the access controller 132 can read the ID, then the access controller 132 determines the new chip is type 2, otherwise the new chip is type 1. In the case of determining that the chip is type 2, the MPU determines a first chip area of the new flash EEPROM as an area for exchanging the exchanged chip, and determines the second chip area as an area for expanding memory area (step S35). The access controller 132 copies all information stored in the exchanged chip (for example, flash EEPROM 101), into the first chip area of the new flash EEPROM connected to the slot 111 (step S36). The MPU rewrites the rewrite count information in the new flash EEPROM to initialize a value '0', because the controller copied the rewrite count information of the exchanged flash EEPROM chip into the new flash EEPROM chip, in the previous copy operation (step 37). Next, the MPU writes the address conversion table 150, to correct the chip number registered physical address to the chip number of the new flash EEPROM chip. Moreover, the MPU enters the second chip area in the address conversion table (step 38). For example, when the number of the new chip connected to the slot 111 is 7, the address conversion table 150 of the Fig. 1 is corrected to change the registered chip number '1' into the chip number '7'. Further, the address conversion table 150 next lists the second chip area as a new logical area. Now, the chip number of the second chip area is #7, but the head address of the second chip area is the next address after the last address of the first chip

area. Next, in response to the MPU signaling an end of the exchanging op ration to the host system, the host system 1 displays a message indicating the end of the exchanging operation (step 39). The user removes the exchanged flash EEPROM chip, after receiving the message from the host system (step 40).

Fig.8 shows a flow chart for expanding flash EEPROM chip memory without exchanging flash EEPROM chips. Hereinafter,the semiconductor memory system has only flash EEPROMs 101-103 as drive #0, and will handle a new expanded flash EEPROM chip or chips as drive #1.

The user inserts a new flash EEPROM chip in to an empty slot, for example the slot 111 (step 51). Next, as a result of the host system being turned on by the user, the MPU in the access controller 132 knows the number of the chips in the semiconductor memory system (step 52). The number of chips can be determined by referring to each Ready/Busy signal line. Next, when the MPU determines it is necessary to expand the memory by comparing the number of chips determined to be connected by the Ready/Busy signals, with the number of chips registered in the config. table, the MPU assigns the expanded chip as drive #1 (step 53). The MPU enters logical addresses assigned as drive #1 in the address conversion table 141 (step 54). After this, the MPU rewrite the number of the chips stored in the config. table to include the new value of the expanded flash EEPROM chip (step 55). As a result, the host system 1 handles the semiconductor memory system 100 as two disk devices corresponding to the drives # 0 and 1.

Further, the semiconductor memory system 100 can not only add to the number of drives, but also can expand memory capacity of the drive 0 or drive 1 by expanding the flash EEPROM chip. For example, in the case of increasing memory capacity of drive #1, the access controller 132 will assign the new logical address following the last logical address in the drive #1 to the new chip.

Accordingly, the semiconductor memory system can exchange memory area of one independent drive, according to replacing and expanding (or reducing) EEPROM chips.

Fig.9 shows yet another embodiment of the present invention.

The semiconductor disk LSI 300 is structured as a single package. The semiconductor disk LSI 300 comprises a flash EEPROM unit 360, a controller unit 330, a host interface 320, a memory command interface 321, memory data interface 322, and chip enable (CE) interface 323.

The flash EEPROM unit 360 comprises an EEPROM cell array and a plurality of peripheral logics, such as a row address d coder,for the cell array. The flash EEPROM unit 360 has an input/output (I/O) register, for example structured 256 byte. In the flash EEPROM unit 360, a minimum unit of data amount handled in a write or an erase operation is determined and the unit amount of data is handled together. For example, it is assumed that the flash EEPROM unit 360 allows data write operations in pages of 256 bytes and data erase operations in blocks of 4K bytes.

The controller unit 330 comprises a host interface controller 331, an access controller 332 and a DRAM 333.

The host interface controller 331 and the DRAM 333 have functions the same as the host interface controller 131 and the DRAM 133 as shown Fig.1.

The host interface 320, like a hard disk drive connectable to the host system 1, has, for example, a 40-pin arrangement conforming with the IDE interface, or like an IC card installable in an IC card slot, has, for example, a 68-pin arrangement conforming with the PCMCIA interface.

The memory command interface 321, the memory data interface 322 and the chip enable interface 323 provide access control of expansion flash EEPROM chips, and each interface 321-323 has a plurality of input/output pins for receiving and transferring each signal between each interface 321-323 and expansion flash EEPROM chips 401-403.

The access controller 332 provides access control of the flash EEPROM unit 360 via the host interface 320 and the host interface controller 331, in response to a disk access request supplied from a host system 1.

There is described a method by which the access controller 332 controls access to the flash EEPROM unit 360.

First, the access controller 332 provides chip enable (CE) signal 0 for indicating an active state to the flash EEPROM unit 360. Next, the access controller 332 provides a command for indicating an operation mode (write,read,erase,verify and so on) to the flash EEPROM unit 360 via the read/write control line. Next, the access controller 332 provides a memory address for indicating an access start address to the flash EEPROM unit 360 via the I/O bus. After providing the memory address, if the operation mode is the write mode, then the access controller 332 transfers write data via the I/O bus, and if the operation mode is the read mode, then the access controller 332 receives read data from the flash EEPROM unit via the I/O bus. Here, if the operation mode is the write mode, the access controller 332 releases access control for flash EEPROM unit 360 after transferring write data to the I/O register in the flash EEPROM unit 360, and the write operation is run automatically by the flash EEPROM unit 360 itself.

The access controller 332 not only can control the flash EEPROM unit 360 in the semiconductor LSI 300, but also can provide the same access control to a plurality of expansion flash EEPROM 401-403 chips connect d to th semiconductor LSI 300, according to need.

Referring to Fig.10, a semiconductor memory system structured by a unit which includes the semiconductor disk LSI 300, such as a memory board and a memory card will be described.

A semiconductor memory system unit 420 is structured by a printed circuit board 410 or which the semiconductor disk LSI 300 and three flash EEPROM chips 401-403 are mounted. Each flash EEPROM chip 401-403 is connected to the memory command interface 321 via a common read/write control line, and is connected to the memory data interface 322 via a common I/O bus. Each flash EEPROM chip 401-403 independently is connected to the chip enable interface 323 via a chip enable signal line and a ready/busy signal line (not shown), and receives the chip enable signal from the chip enable interface 323. Moreover, the semiconductor memory system unit 420 has a card edge type connector 430 for connecting between the host system 1 and the host interface 320 in the semiconductor disk LSI 300.

In response to generating one of the chip enable signals CE1-3, one of the expansion flash EEPROM chips 401-403 is selected. Hereinafter, CE1,CE2 and CE3 are used for selecting each expansion flash EEPROM chip. In the case of selecting the expansion flash EEPROM chip 401, CE 1 is generated. Similarly, in the case of selecting the expansion flash EEPROM chip 402, CE 2 is generated. Similarly, in the case of selecting the expansion flash EEPROM chip 403, CE 3 is generated.

The chip enable signal is generated by the access controller 332, on the basis of an address conversion table 350, as shown Fig.11.

The address conversion table 350 defines the relation between logical addresses and physical address. The logical addresses has a track (cylinder + head) number and a sector number. The physical address has a chip number and a memory address. The chip number is used for determining the chip enable signal.

If the access controller 332 receives a logical address between track number 0 and L, then the address conversion table 350 indicates chip enable signal 0 (CE 0) should be generated for selecting internal flash EEPROM unit 360. Similarly,if access controller 332 receives a logical address between track number L+1 and 2L, the address conversion table 350 indicates chip enable signal 1 (CE 1) should be generated for selecting the first expansion flash EEPROM chip 401. Similarly,if access controller 332 receives a logical address between track number 2L+1 and 3L, the address conversion table 350 indicates chip enable signal 2 (CE 2) should be generated for selecting the second xpansion flash EEPROM chip 402. Similarly,if access controller 332 receives a logical address between track number 3L+1 and 4L, the address conversion table 350 indicates chip nable signal 3 (CE 3) should be generated for selecting the third expansion flash EEPROM chip 403.

Thus, the semiconductor disk LSI 300 can be structured as a single chip which can control the internal flash EEPROM and the expansion EEPROM chips.

Therefore, a semiconductor memory system 420 including the semiconductor disk LSI 300 is able to reduce the number of parts and to achieve miniaturization and low-cost.

When the semiconductor memory system 420 is used by the host system 1, the host system 1 further is able to assign the semiconductor memory system unit 420 to two disk drives, as in the above embodiment. This concept is shown by Fig. 12.

The host system 1 assigns a first memory block 500 (the flash EEPROM unit 360) the drive number 0, and assigns a second memory block (the expansion flash EEPROM 401-403) the drive number 1. That is, the host system 1 recognizes the semiconductor memory system 420 as two different secondary memories. The semiconductor disk drive LSI 300 manages each memory block independently, according to each MBIT (memory block information table) 491, 494, 495, 496. Moreover, the flash EEPROM chips 401-403 can be connected to the printed circuit board via a slot, in the same manner as IC slots 201-203 as shown in fig.3.

Thus, a user can expand memory capacity in the semiconductor memory system unit easily, according to need.

The following describes an embodiment of a semiconductor memory system which uses the semiconductor disk LSI 300 as shown fig 9 through fig 12 as secondary memory in a personal computer.

Fig.13 and Fig.14 show a host system 600 connected to a semiconductor memory system, which is a memory board type.

A CPU 611, main memory 612, two I/O controller 613, 614, a connector 630, etc., mount on a mother board 610 in the host system 600, and each component is interconnected to a system bus 615. The semiconductor memory system is structured to include a memory board 620 on which is mounted the semiconductor disk LSI 300 and three flash EEPROM chips 401-403. The memory board 620 is connected to the host system 600 via the connector 630. The memory board 620 is also connected to the system bus 615. Moreover, the memory board 620 becomes memory card, if the memory board 620 is provided as a package.

The following describes another embodiment of a semiconductor memory system which uses the semiconductor disk LSI 300 as secondary memory in a p rsonal computer.

Fig.15 and Fig.16 show a semiconductor memory system, which is structured to include the semiconductor disk LSI 300 and three flash EEPROM chips 401-403 mounted on a mother board 710 in the host

system 600.

A CPU 611, main memory 612, two I/O controllers 613, 614, etc., are mounted on the mother board 710 in the host system 600, and each component is interconnected to the system bus 615. Each of the semiconductor disk LSI 300 and three flash EEPROM chips 401-403 for structuring the semiconductor memory system can be handled as a peripheral chip, such as the CPU chip 611, and can be connected to the system bus 615 directly.

The mother board 710 in the host system 600 does not have to have a connector for a memory card or a memory board. Therefore, a mounting layout on the mother board 710 is more flexible.

Fig. 17 illustrates a physical arrangement of the mother board 710.

A LSI slot 720 and IC slots 721-723 are directly mounted on the mother board 710, but the semiconductor disk drive LSI 300 is mounted on the mother board 710 via the LSI slot 720 and the flash EEPROM chips 401-403 are mounted on the mother board 710 via the IC slots 721-723.

Therefore, the mother board adds only four slots 720-723 and lines for interconnecting to each slot, because the semiconductor disk drive LSI 300 and each flash EEPROM chip 401-403 can easily be connected and disconnected by the user. Therefore, the user can select whether the semiconductor memory system is introduced in the personal computer 600 freely.

Further, with reference to Fig.18, the host interface 320 in a semiconductor disk LSI 300 may have a signal ID in the case of mounting the semiconductor disk drive LSI 300 on the mother board 710. The signal ID indicates whether the semiconductor disk drive LSI 300 is connected to the LSI slot 720. The signal ID is provided as a high active state by an electrical charge terminal for keeping the high active state. Generally speaking, a magnetic disk interface had by a host system uses the ID signal, for determining whether the magnetic disk drive is connected to the host system. Thus, the magnetic disk interface can be used without exchanging the magnetic disk interface had by the host system.

Claims

1. A periperal semiconductor memory system including first and second memory drives, comprising:

   a first flash EEPROM (181) included in the first memory drive;

   a second flash EEPROM (182) included in the second memory drive;

   means for controlling access (132) to the first and second flash EEPROMs (181, 182) including addr ss conv rting means for converting a logical address from a host system (1) into a physical address, according to first and second file manag ment information (150) which indicates correspondence between logical addresses and physical addresses of the first and second memory drives,respectively; and

   the access controlling means (132) further including memory accessing means, coupled to each of the first and second flash EEPROMs (181, 182), for accessing a selected EEPROM according to the physical address from said address converting means.

2. The semiconductor memory system according to claim 1, wherein the first memory drive stores the first file management information (191, 192, 193), and the second memory drive stores the second file management information (194, 195, 196).

3. The semiconductor memory system according to claim 1, further comprising a temporary memory, wherein the first and second file management information (150) is stored in the temporary memory (133).

4. The semiconductor memory system according to claim 1, wherein the first and second EEPROMs and the access controlling means (132) are mounted on a mother board (710) in the host system (600).

5. The semiconductor memory system according to claim 1, wherein the first and second EEPROMs (181, 182) are provided as first and second flash EEPROM chips (101, 102, 103, 104, 105, 106);

   the memory system further comprising slots (201, 202, 203, 204, 205, 206) for removably connecting the first and second flash EEPROM chips (101, 102, 103, 104, 105, 106).

6. The semiconductor memory system according to claim 1, wherein the first and second EEPROMs (181, 182) are provided as first and second flash EEPROM chips (101, 102, 103, 104, 105, 106);

   the memory system further comprising a slot (111) for removably connecting another flash EEPROM chip.

7. The semiconductor memory system according to claim 6, the memory system further comprising slots (201, 202, 203, 204, 205, 206) for removably connecting the first and second flash EEPROM chips (101, 102, 103, 104, 105, 106).

8. A method of managing a semiconductor memory device (100) as drives managed by a host system (1), wherein the semiconductor m mory device (100) has a plurality of flash EEPROM chips

(101, 102, 103, 104, 105, 106) and a controller (132) for controlling the plurality of flash EEPROM chips in response to a request for access from the host system (1), comprising steps of:

managing at least a first one of the plurality of flash EEPROM chips (101, 102, 103) as included in a memory area of a first drive, in accordance with first file management information (191, 192, 193) which indicates correspondence between logical addresses and physical addresses;

managing at least a second one of the plurality of flash EEPROM chips (104, 105, 106) as included in a memory area of a second drive, in accordance with second file management information (194, 195, 196) which indicates correspondence between logical addresses and physical addresses; and

selectively controlling the first and second drives according to a physical address converted from a logical address from the host system in accordance with the first file management information (191, 192, 193) and the second file management information (194, 195, 196).

9. A method of claim 8, further comprising steps of:

removing one of the flash EEPROM chips (101, 102, 103) included in the memory area of the first drive; and reformatting the memory area of the first drive.

10. A method of claim 8, further comprising the steps of:

removing one of the flash EEPROM chips (101, 102, 103) included in the memory area of the first drive;

connecting a new flash EEPROM chip to the controller (132);

managing the new flash EEPROM chip as included in the first memory drive; and

reformatting the memory area of the first drive.

11. A method of claim 8,wherein the semiconductor memory device has a slot, connected to the controller, further comprising the steps of:

inserting a new flash EEPROM chip into the slot,

copying data from a selected chip included in memory area of the first drive into the new flash EEPROM chip; and

reassigning the new EEPROM chip as included in the memory area of the first drive.

12. A method of claim 11, wherein the selected one of the flash EEPROM chips (101, 102, 103) has a rewrite counter for counting a number of rewrite times of the selected flash EEPROM chip, further comprising the step of:

r writing a value of the rewrite counter to '0' in the new EEPROM chip.

13. A method of claim 8, further comprising steps of:

removing a selected one of the flash EEPROM chips (101, 102, 103) included in the memory area of the first drive;

installing a new flash EEPROM chip which has a memory capacity greater than the selected one of the flash EEPROM chips (101, 102, 103); and

assigning in the new flash EEPROM chip a replacement memory area substantially equal in capacity to the memory capacity of the selected one of the flash EEPROM chips (101, 102, 103), and an expansion memory area of the first drive having a capacity substantially equal to a remaining portion of the new flash EEPROM chip.

14. A method of exchanging a flash EEPROM chip in a semiconductor memory device (100), wherein the semiconductor memory device (101) has a plurality of flash EEPROM chips (101, 102, 103, 104, 105, 106) and a controller for controlling the plurality of flash EEPROM chips (101, 102, 103, 104, 105, 106) in response to request for access from a host system (1), and a number of rewrite times of flash EEPROM, comprising steps of:

connecting a new flash EEPROM chip to the controller;

copying data from one plurality of flash EEPROM chips (101, 102, 103, 104, 105, 106) into the new flash EEPROM chip; and

rewriting a value of the rewrite counter to '0' in the new flash EEPROM chip.

15. A method of handling memory using in a peripheral semiconductor memory system (100) having a first memory drive and a second memory drive,comprising the steps of:

managing the first memory drive in accordance with first file management information (191, 192, 193) which indicates a correspondence between logical addresses and physical addresses of the first memory drive;

managing the second memory drive in accordance with second file management information (194, 195, 196) which indicates a correspondence between logical addresses and physical addresses of the second memory drive;

converting in a common memory access controller (132) a logical address from a host system into a physical address according to the first management information (191, 192, 193) and second file management information (194, 195, 196); and

accessing one of the first and second memory drives according to th physical address converted from the logical address.

16. A semiconductor memory system comprising:
flash EEPROM unit (360) having a flash EEPROM cell array and peripheral logic for controlling the cell array;
a controller (332) for controlling the flash EEPROM unit and an external flash EEPROM chip (401, 402, 403), coupled to a control line for transferring a memory command to the flash EEPROM unit, an input/output bus for transferring a memory address and data and a first select line for selecting the flash EEPROM unit;
a host interface (320) for communicating with a host system (1);
a command interface (321) connected to the control line for communicating to the external flash EEPROM chip (401, 402, 403);
a data interface (322) connected to the input/output bus for communicating to the external flash EEPROM chip (401, 402, 403); and
a chip enable interface (323) connected to a second select line for selecting the external flash EEPROM chip (401, 402, 403);
wherein, components of the memory system are configured as one package, and said controller (332) controls the external flash EEPROM chip by selecting the second select line.

17. The semiconductor memory system according to claim 16, wherein, the semiconductor memory system is mounted on a mother board (710) in the host system (600).

18. A semiconductor memory system comprising:
an external flash EEPROM chip (401); and
a semiconductor disk LSI (300), housed by one package, the semiconductor disk LSI (300) including:
a flash EEPROM unit (360) having a flash EEPROM cell array and peripheral logic for controlling the cell array;
a controller for controlling the flash EEPROM unit (360) and the external flash EEPROM chip (401) coupled to a control line for transferring a memory command to the flash EEPROM unit (360) , an input/output bus for transferring a memory address and data and a first select line for selecting the flash EEPROM unit (360);
a host interface (320) for communicating to a host system (1);
a command interface (321) connected to th control line for communicating to the external flash EEPROM chip;
a data interface (322) conn ct d to the input/output bus for communicating to the external flash EEPROM chip (401); and
a chip enable interface (323) connected to a second sel ct line for selecting the external flash EEPROM chip (401);
wherein a first memory block (500) includes a memory area of the flash EEPROM unit (360) and is managed in accordance with first file management information (491) which indicates correspondence between logical addresses and physical addresses;
wherein a second memory block (510) includes a memory area of the external flash EEPROM chip (401) and is managed in accordance with second file management information (494) which indicates correspondence between physical addresses and logical addresses;
means for controlling access to the flash EEPROM unit (360) and external flash EEPROM chip (401) including address converting means converts a logical address, from the host system (1) into a physical address, according to one of the first file management information (491) and the second management information (494);
the access controlling means further including memory accessing means, coupled to the flash EEPROM unit (360) and the external flash EEPROM chip (401), for accessing a selected EEPROM according to the physical address from said address converting means.

19. The semiconductor memory system according to claim 18, further including a second external flash EEPROM chip, wherein the first memory block further includes a memory area of the second external flash EEPROM chip .

20. A semiconductor memory system provided as a secondary memory for a host computer (600), comprising:
a plurality of flash EEPROM chips (401, 402, 403); and
a controller (300) connected to each of the flash EEPROM chips for controlling each of the flash EEPROM chips (401, 402, 403), according to requests for disk access from a host system (600);and
wherein the semiconductor memory system is mountable on a mother board (710) of the host system (600).

21. The semiconductor memory system according to claim 20, further comprising a plurality of slots connected to the controller (300), for connecting to the controller the plurality of flash EEPROM chips(401, 402, 403).

22. The semiconductor memory system according to claim 21, further comprising a controller slot di-

EP 0 613 151A2

rectly connected to the host system (600).

23. The semiconductor memory system according to claim 22, further comprising an ID signal line, for indicating whether the host system (600) is connected to the controller (300).

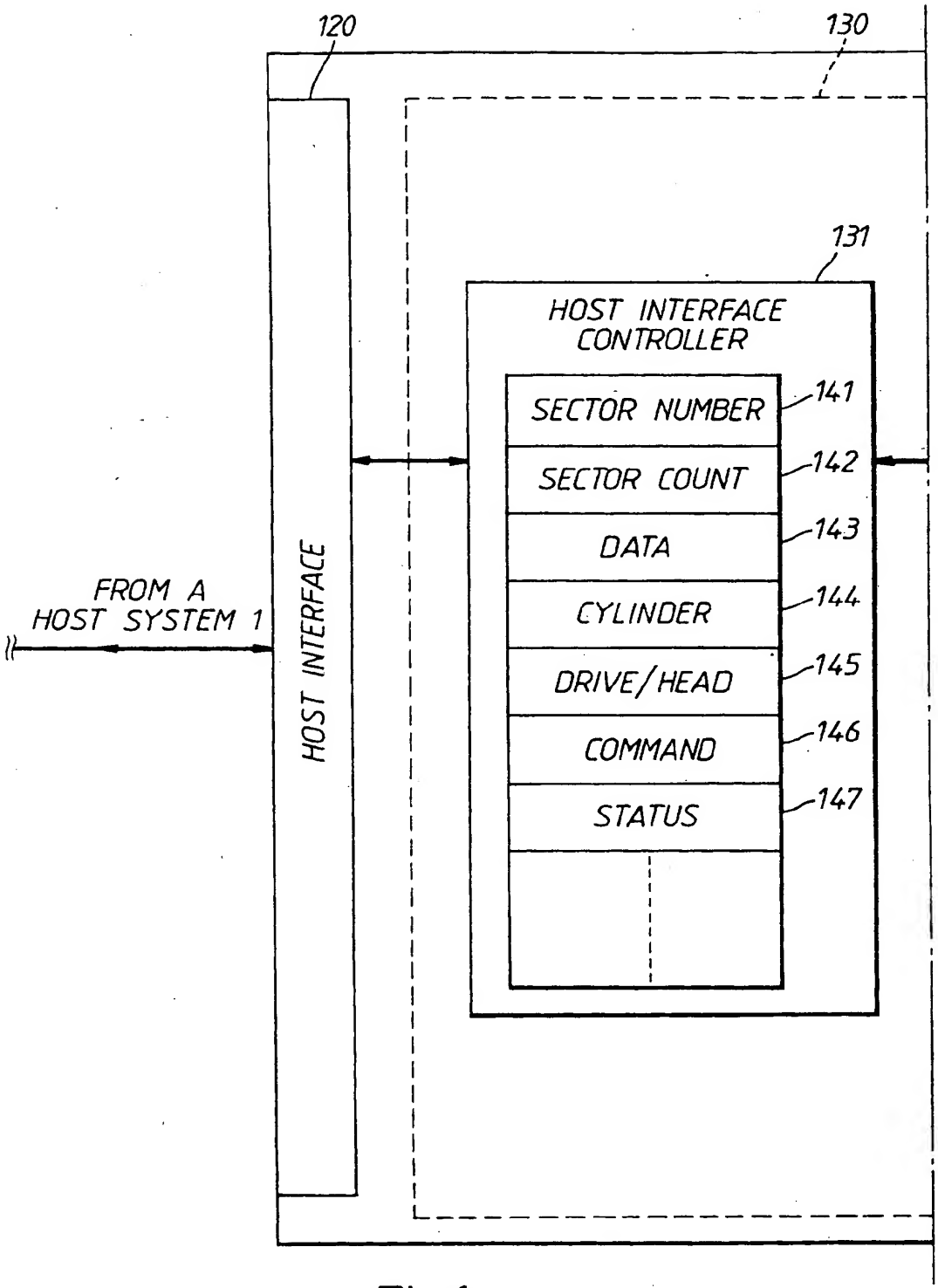


Fig.1a

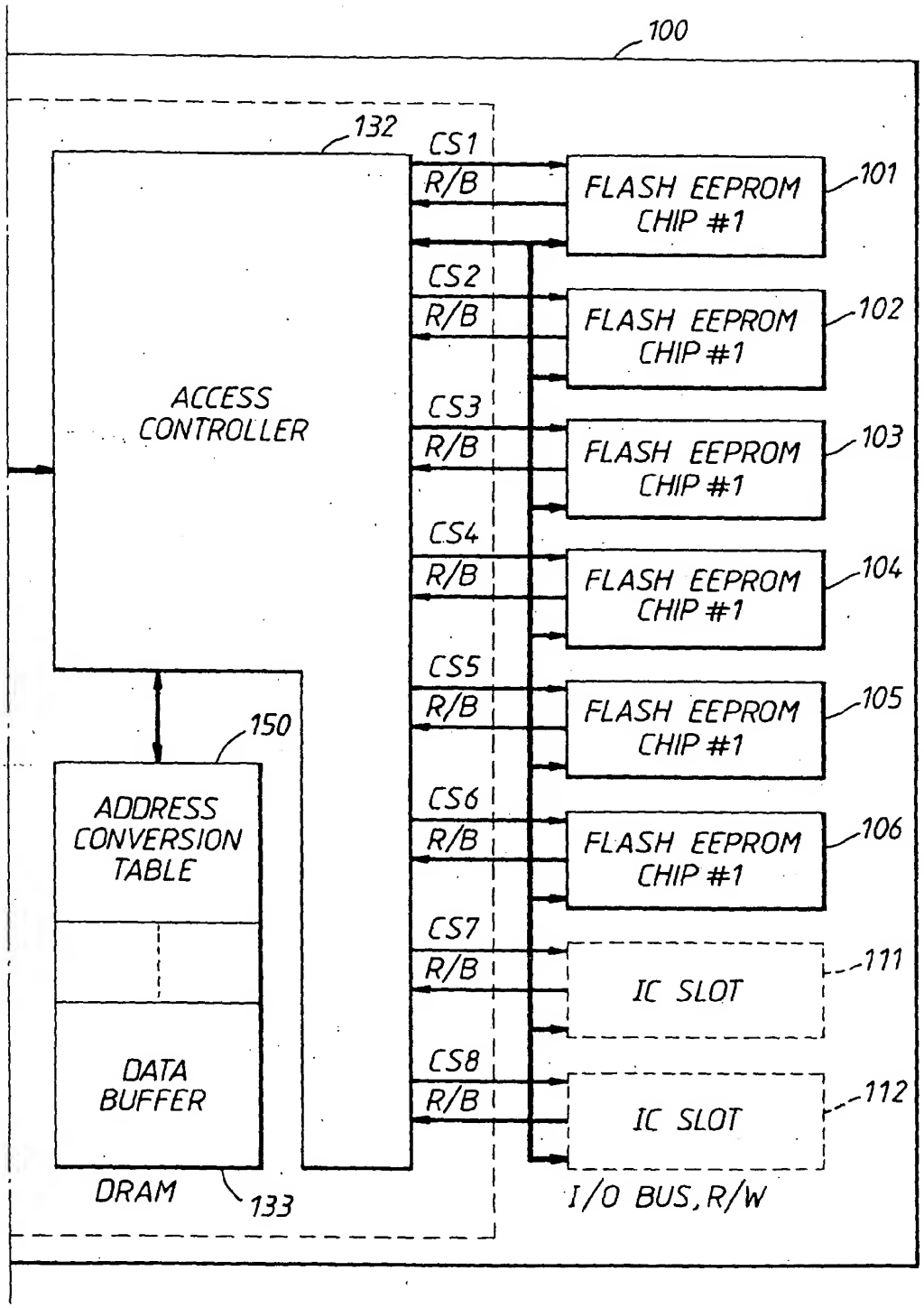

100
132
ACCESS CONTROLLER
150
ADDRESS CONVERSION TABLE
DATA BUFFER
DRAM
133
CS1
R/B
FLASH EEPROM CHIP #1
101
CS2
R/B
FLASH EEPROM CHIP #1
102
CS3
R/B
FLASH EEPROM CHIP #1
103
CS4
R/B
FLASH EEPROM CHIP #1
104
CS5
R/B
FLASH EEPROM CHIP #1
105
CS6
R/B
FLASH EEPROM CHIP #1
106
CS7
R/B
IC SLOT
111
CS8
R/B
IC SLOT
112
I/O BUS, R/W

Fig.1a (cont)

LOGICAL ADDRESS				PHYSICAL ADDRESS	
DRIVE Nr.	CYLINDER	HEAD	SECTOR	CHIP Nr.	MEMORY ADDRESS
# 0			1	# 1	
# 0			2	# 1	
⋮	⋮	⋮	⋮		
# 0				# 1	
# 0				# 2	
⋮	⋮	⋮	⋮		
# 0				# 2	
# 0				# 3	
⋮	⋮	⋮	⋮		
# 0			n	# 3	
# 1			0	# 4	
# 1			1	# 4	
⋮	⋮	⋮	⋮		
# 1				# 4	
# 1				# 5	
⋮	⋮	⋮	⋮		
# 1				# 5	
# 1				# 6	
⋮	⋮	⋮	⋮		
# 1			m	# 6	

Fig. 1b

MEMORY BLOCK INFORMATION TABLE

MEMORY ADDRESS	LOGICAL ADDRESS
0	
1	
2	
n	

191-196

Fig.1c

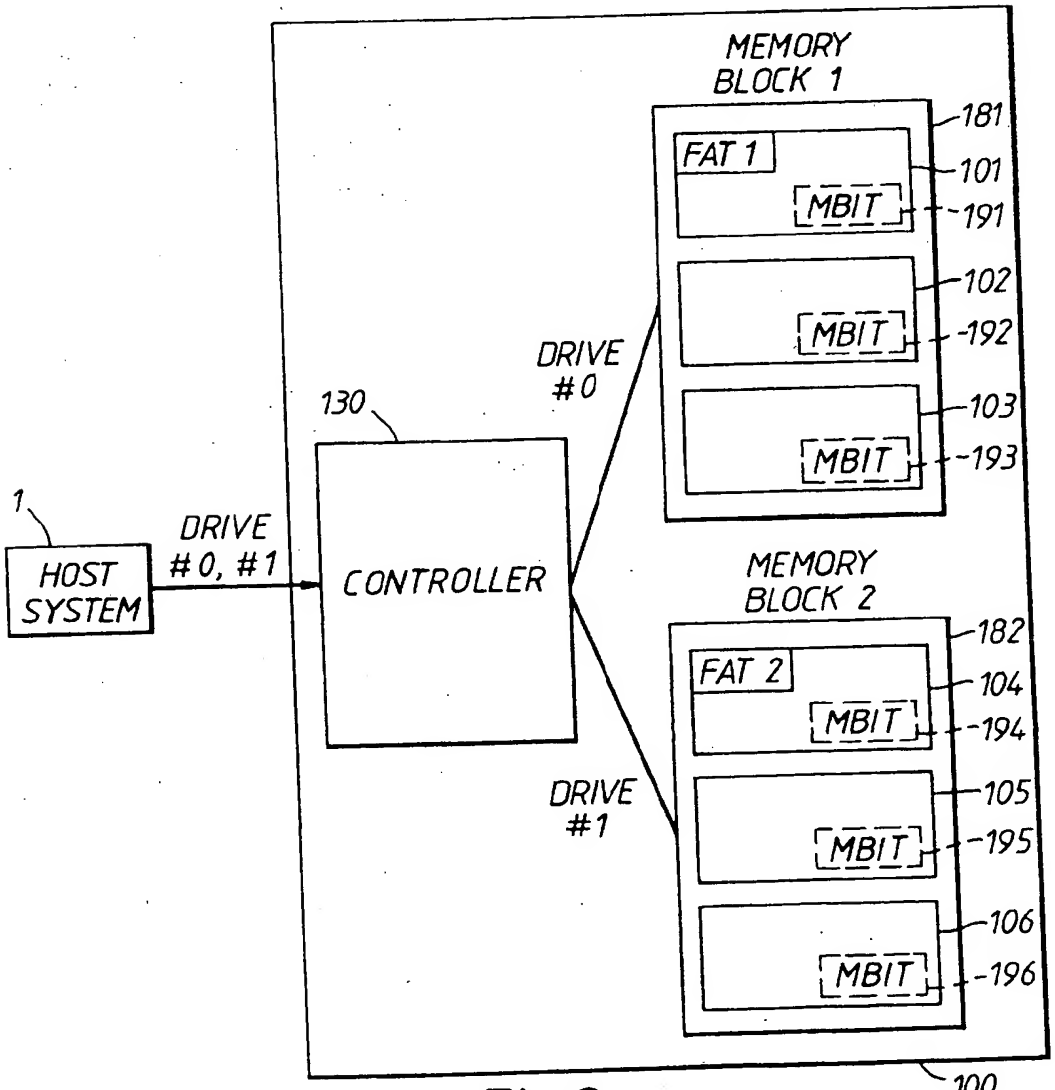


Fig.2

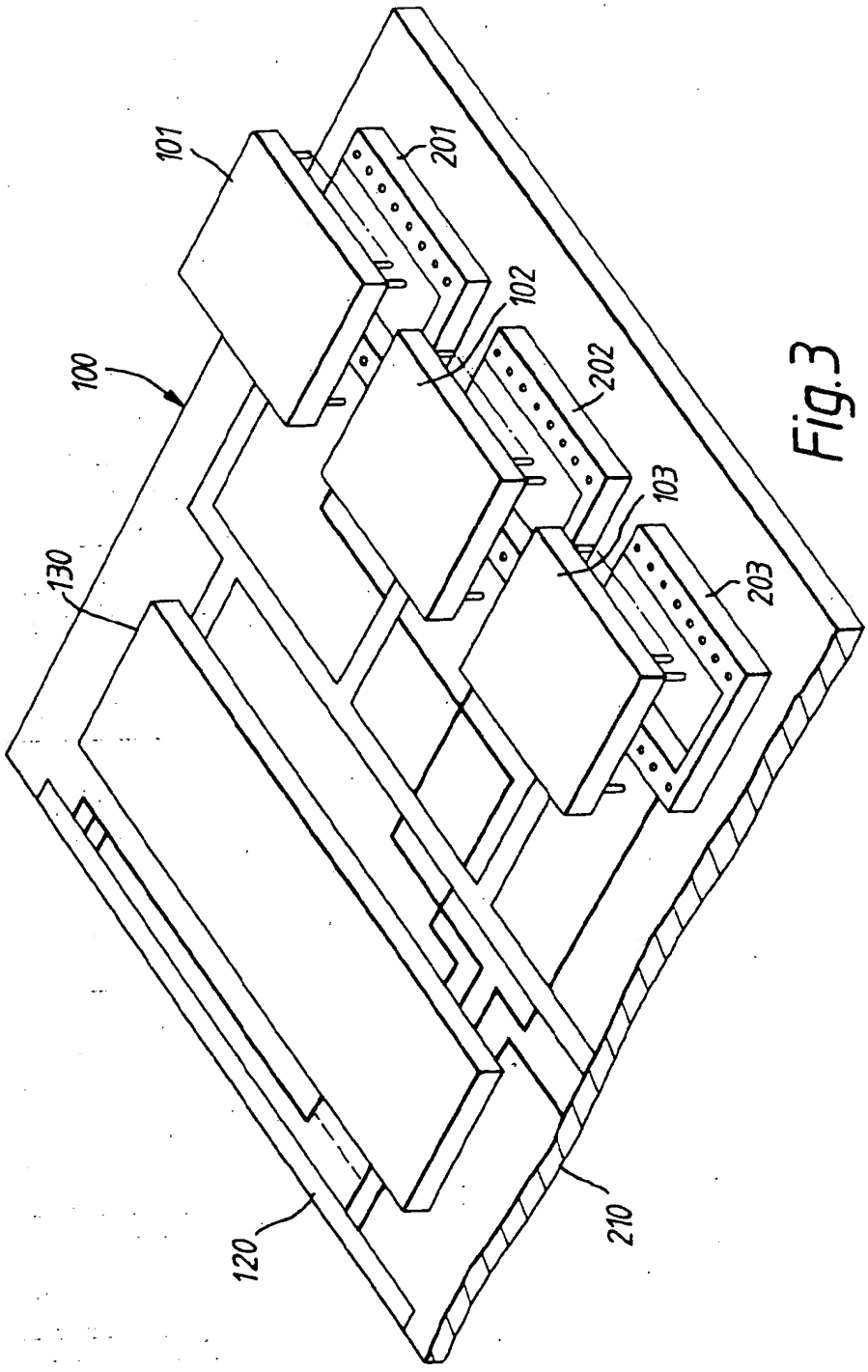


Fig.3

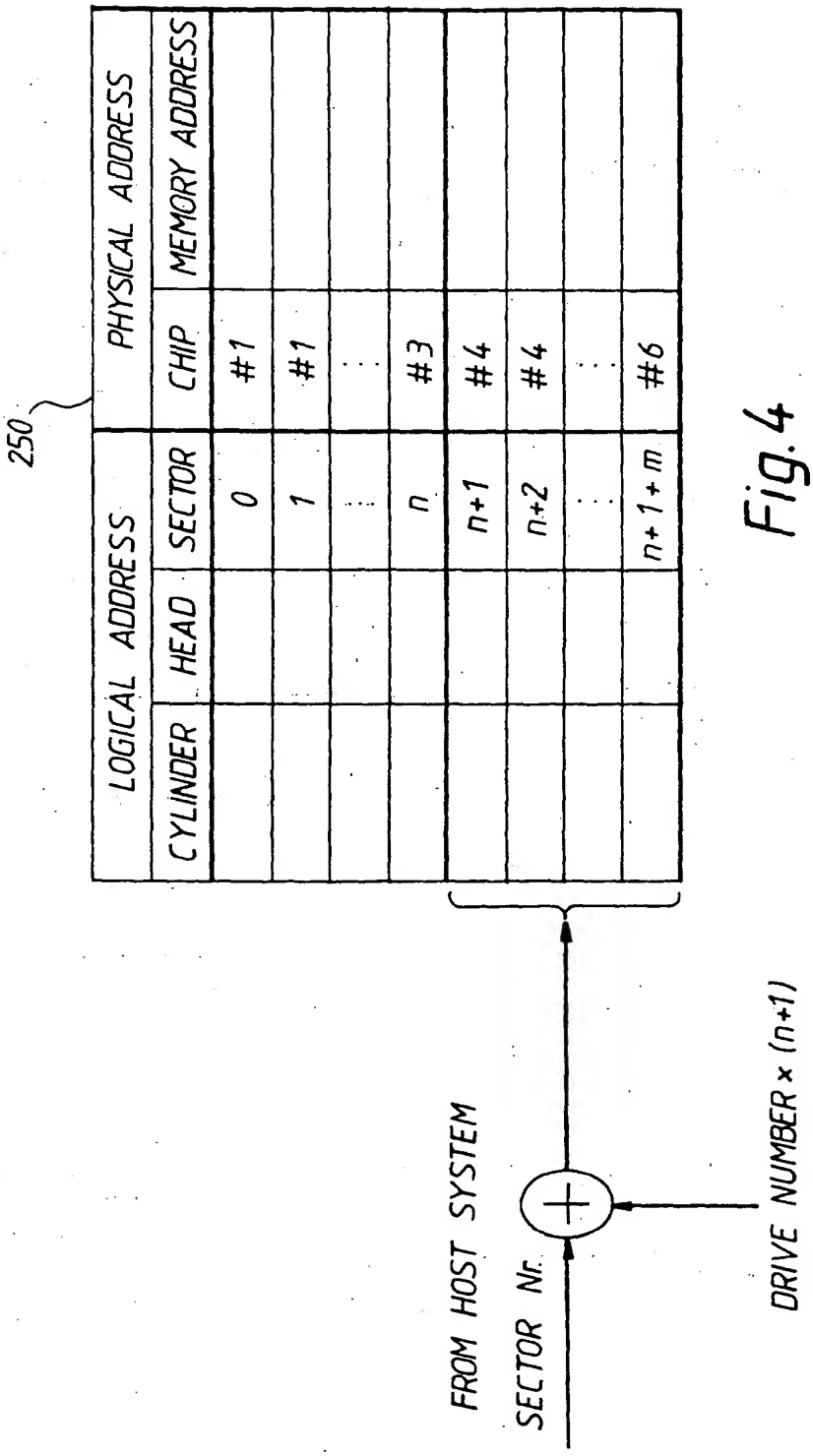

250
LOGICAL ADDRESS
CYLINDER
HEAD
SECTOR
PHYSICAL ADDRESS
CHIP
MEMORY ADDRESS
0
#1
1
#1
n
#3
n+1
#4
n+2
#4
n+1+m
#6
FROM HOST SYSTEM
SECTOR Nr.
DRIVE NUMBER × (n+1)

Fig.4

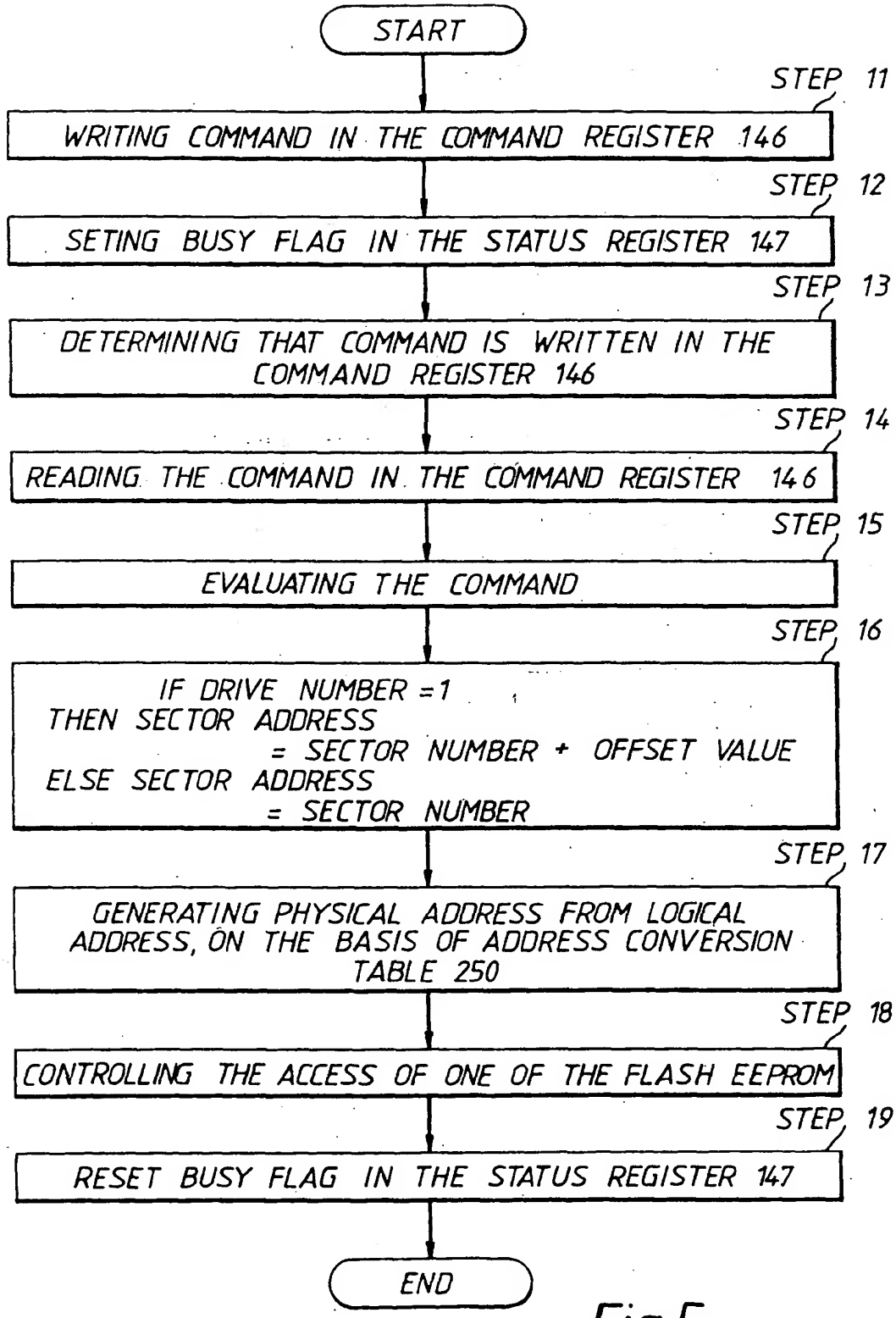

START
STEP 11
WRITING COMMAND IN THE COMMAND REGISTER 146
STEP 12
SETING BUSY FLAG IN THE STATUS REGISTER 147
STEP 13
DETERMINING THAT COMMAND IS WRITTEN IN THE COMMAND REGISTER 146
STEP 14
READING THE COMMAND IN THE COMMAND REGISTER 146
STEP 15
EVALUATING THE COMMAND
STEP 16
IF DRIVE NUMBER = 1
THEN SECTOR ADDRESS
= SECTOR NUMBER + OFFSET VALUE
ELSE SECTOR ADDRESS
= SECTOR NUMBER
STEP 17
GENERATING PHYSICAL ADDRESS FROM LOGICAL ADDRESS, ON THE BASIS OF ADDRESS CONVERSION TABLE 250
STEP 18
CONTROLLING THE ACCESS OF ONE OF THE FLASH EEPROM
STEP 19
RESET BUSY FLAG IN THE STATUS REGISTER 147
END

Fig.5

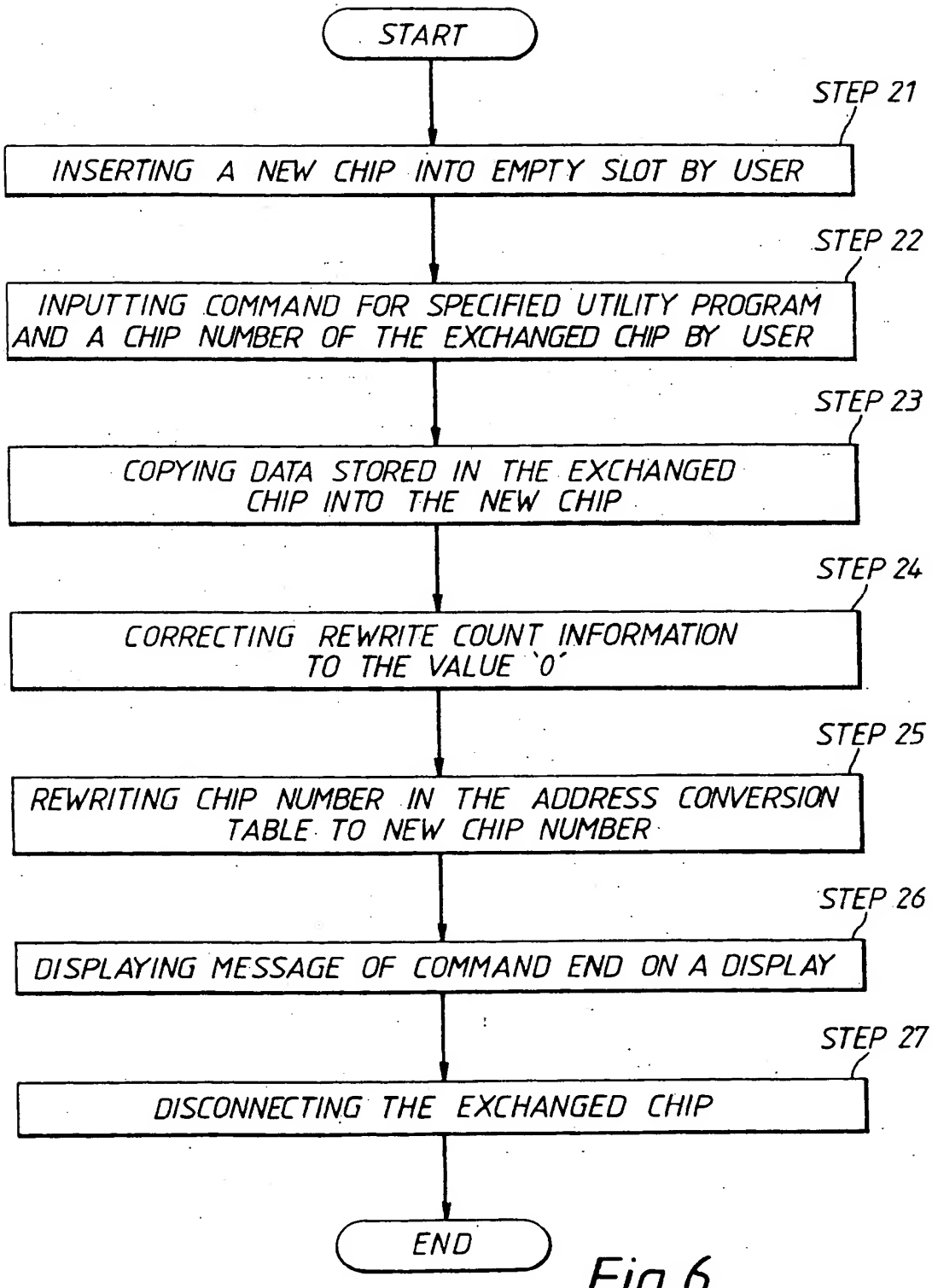


Fig.6

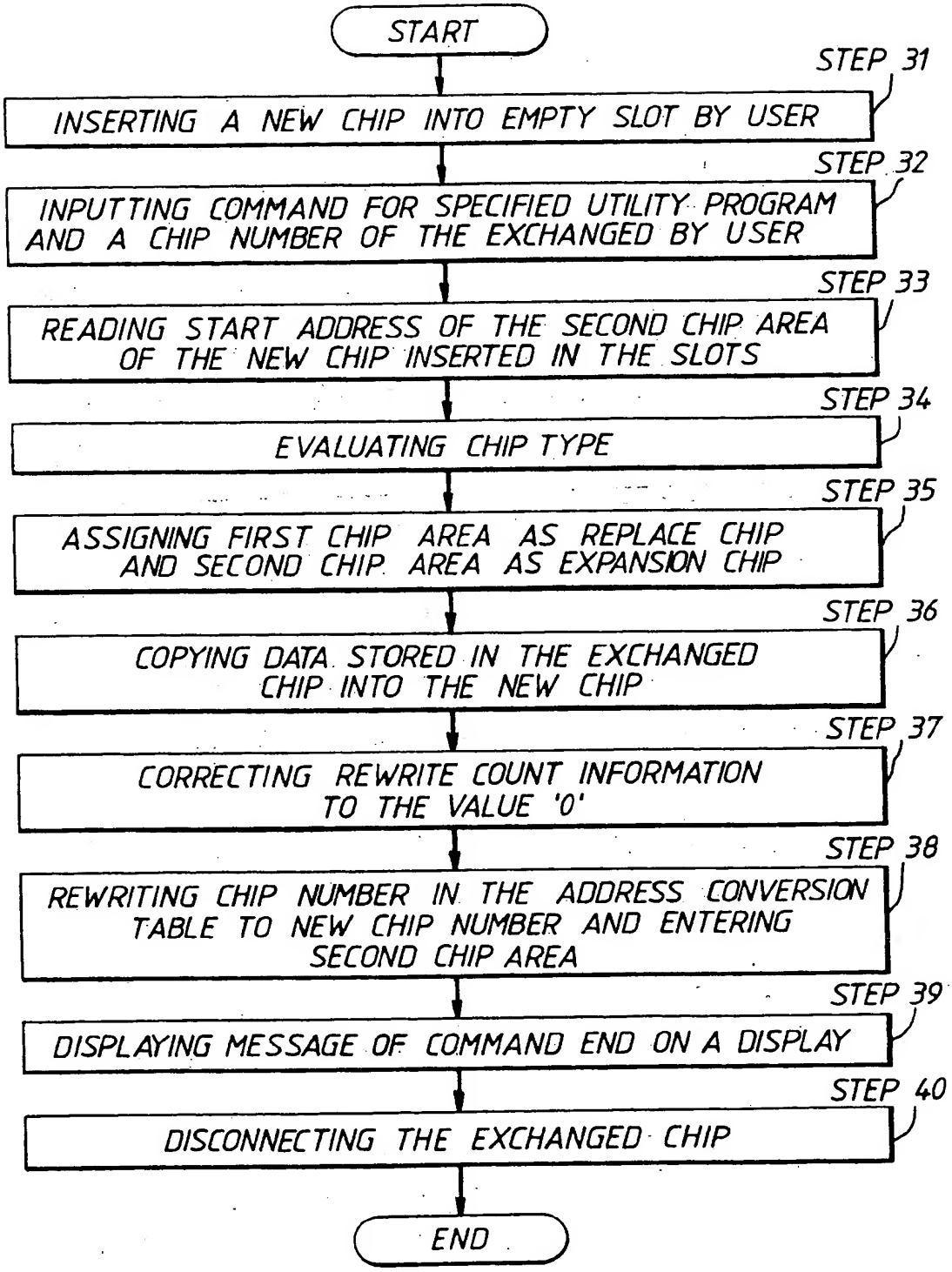


Fig.7

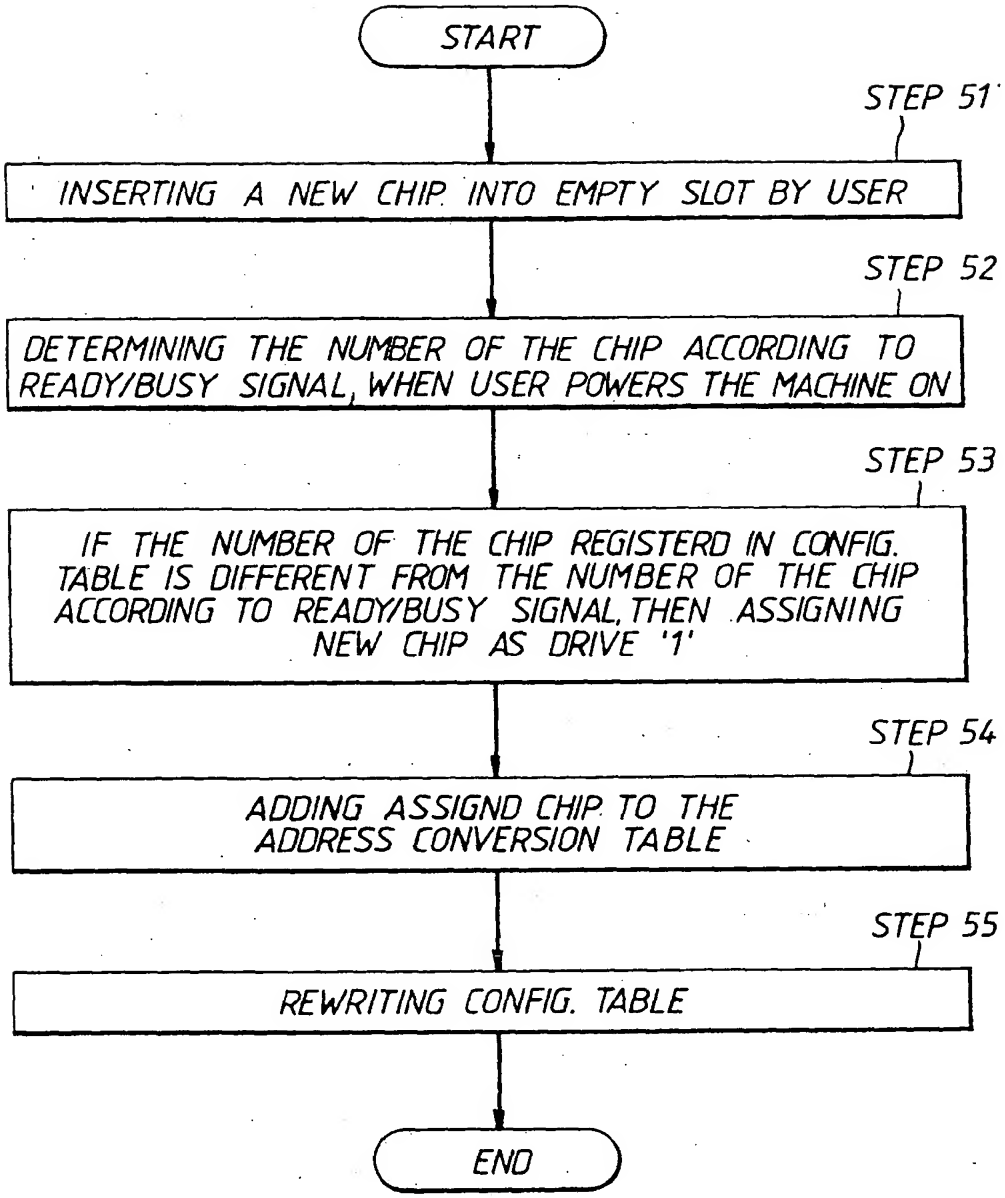


Fig.8

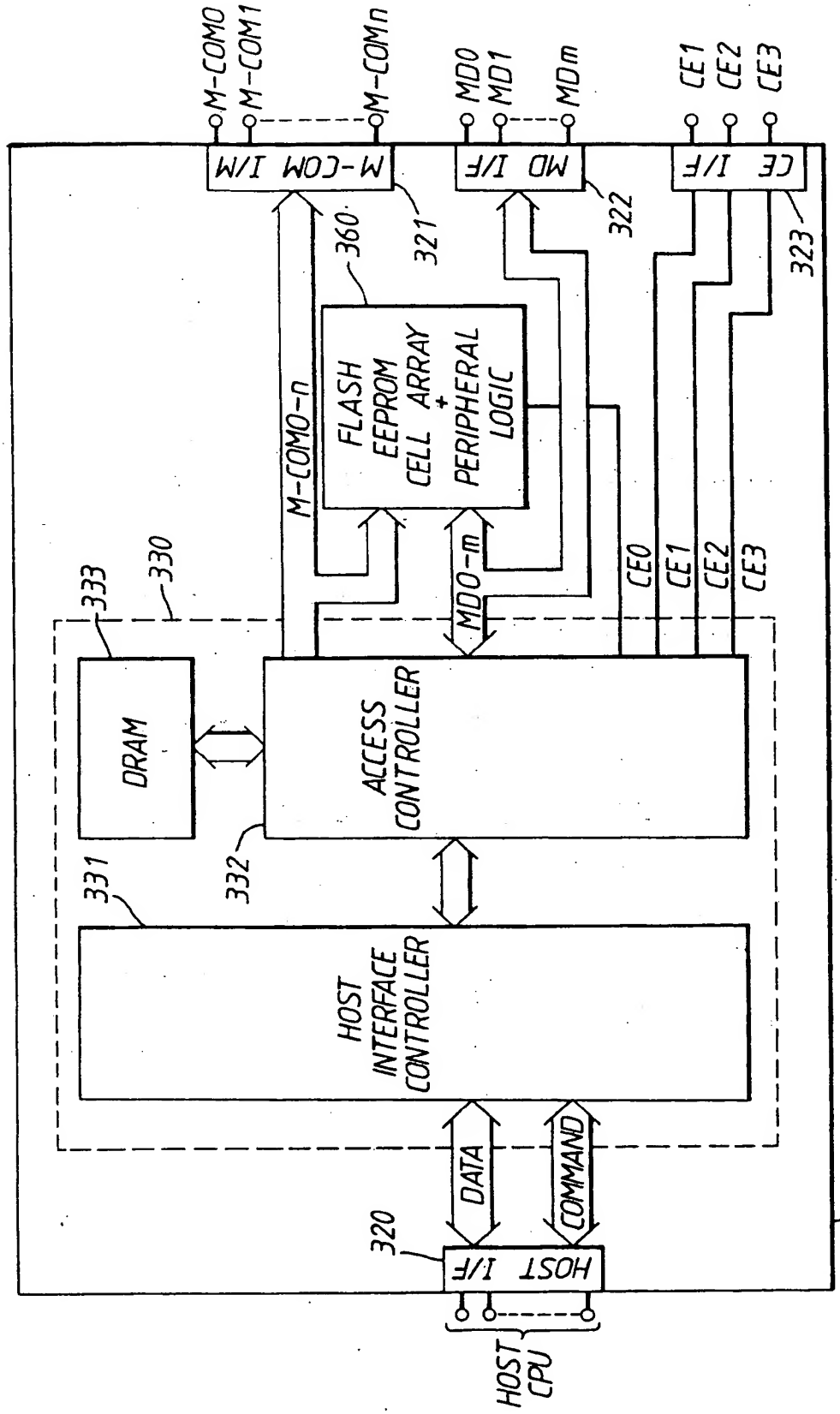


Fig.9

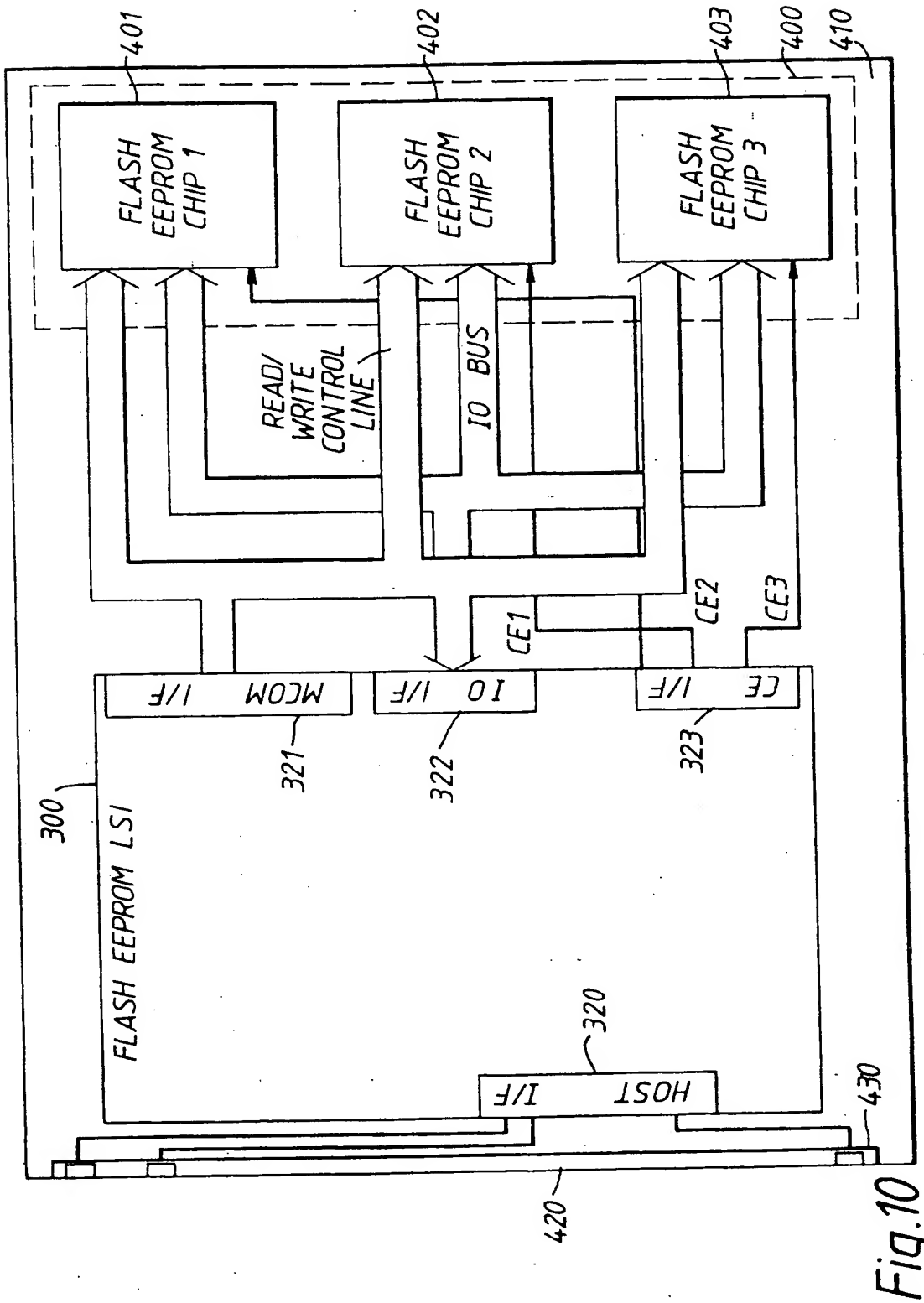

401
402
403
400
410
FLASH EEPROM CHIP 1
FLASH EEPROM CHIP 2
FLASH EEPROM CHIP 3
READ/ WRITE CONTROL LINE
IO BUS
CE1
CE2
CE3
MCOM I/F
IO I/F
CE I/F
321
322
323
300
FLASH EEPROM LSI
320
HOST I/F
430
420

Fig.10

350

ADDRESS CONVESION TABLE

LOGICAL ADDRESS		PHYSICAL ADDRESS		
TRACK No.	SECTOR	CHIP No.	MEMORY ADDRESS	
1 ⋮ L	0 – n ⋮ 0 – n	CE0 ↓		INTERNAL FLASH EEPROM
L + 1 ⋮ 2L	0 – n ⋮ 0 – n	CE1 ↓		EXPANSION FLASH EEPROM 1
2L + 1 ⋮ 3L	0 – n ⋮ 0 – n	CE2 ↓		EXPANSION FLASH EEPROM 2
3L + 1 ⋮ 4L	0 – n ⋮ 0 – n	CE3 ↓		EXPANSION FLASH EEPROM 3

Fig.11

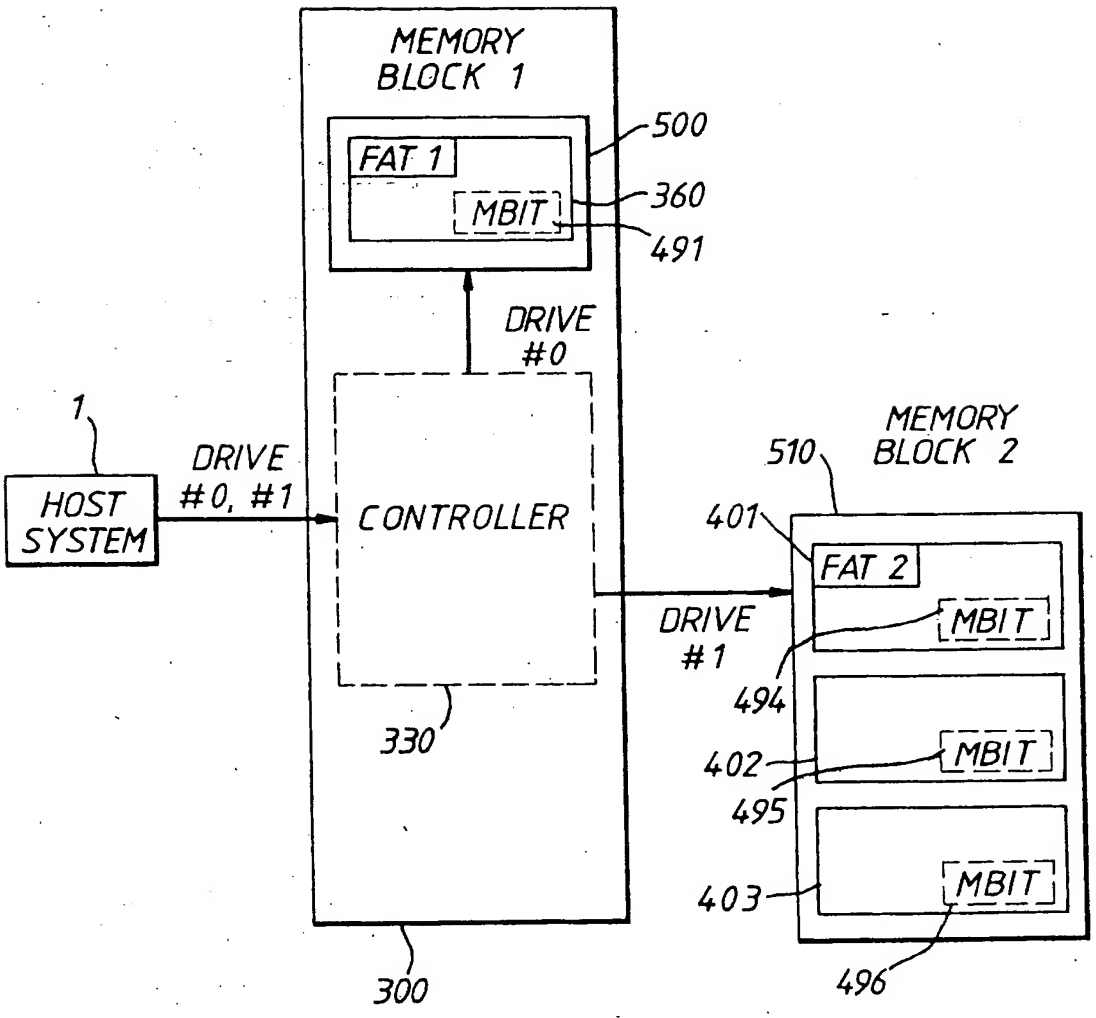

MEMORY
BLOCK 1
FAT 1
MBIT
500
360
491
DRIVE
#0
1
HOST
SYSTEM
DRIVE
#0, #1
CONTROLLER
330
300
MEMORY
BLOCK 2
510
401
FAT 2
MBIT
DRIVE
#1
494
MBIT
402
495
MBIT
403
496

Fig.12

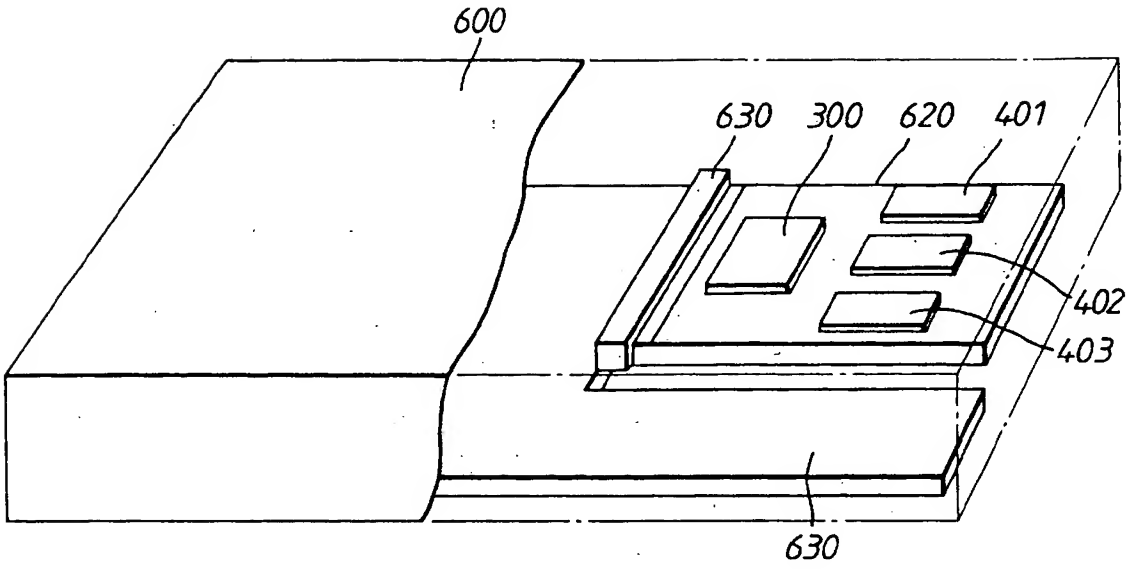


Fig.13

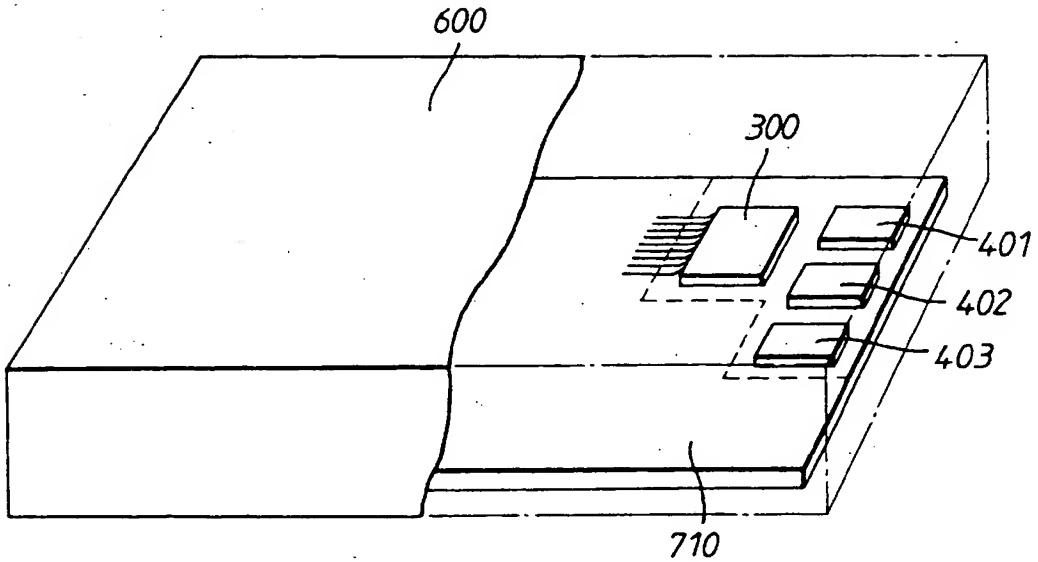


Fig.15

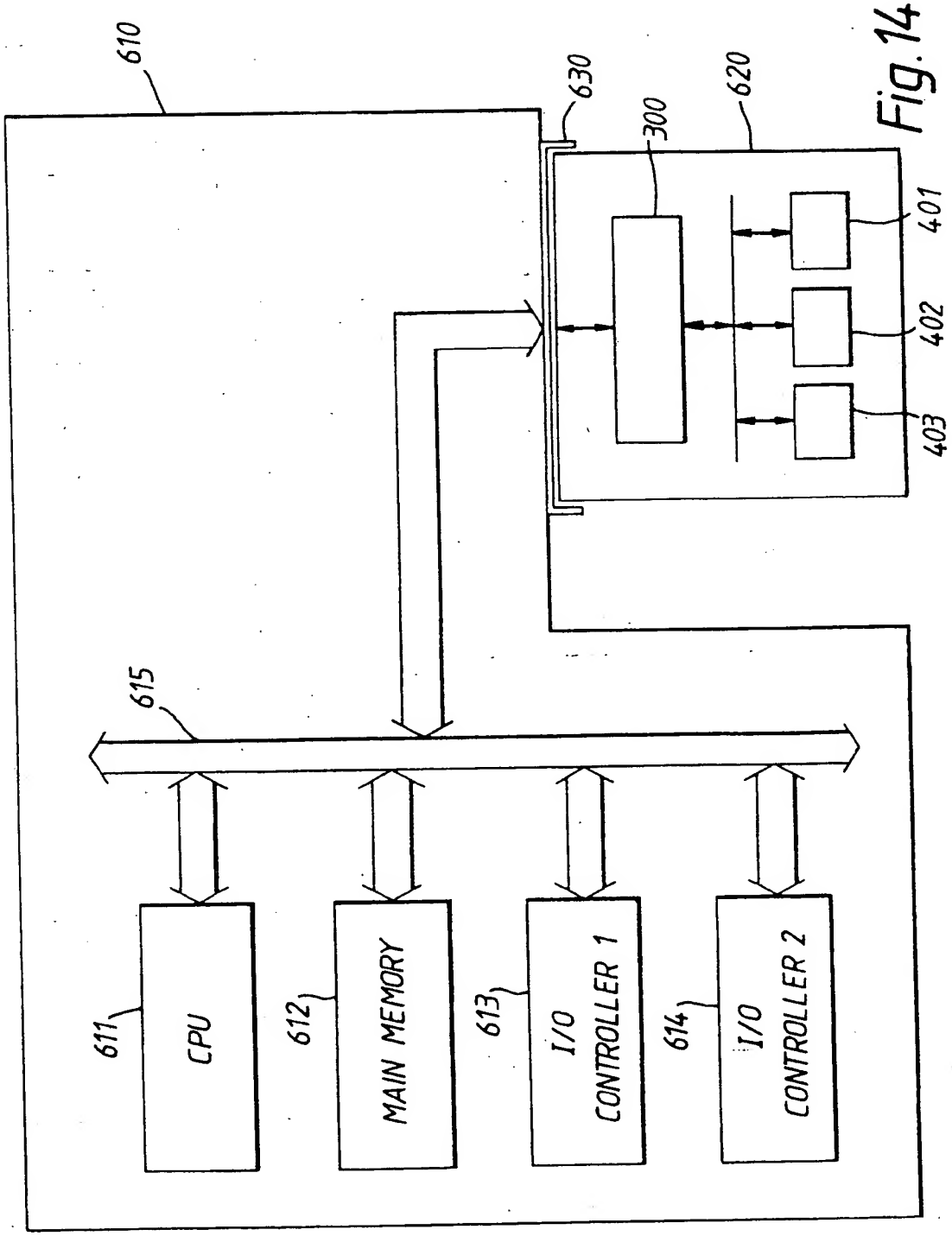


Fig. 14

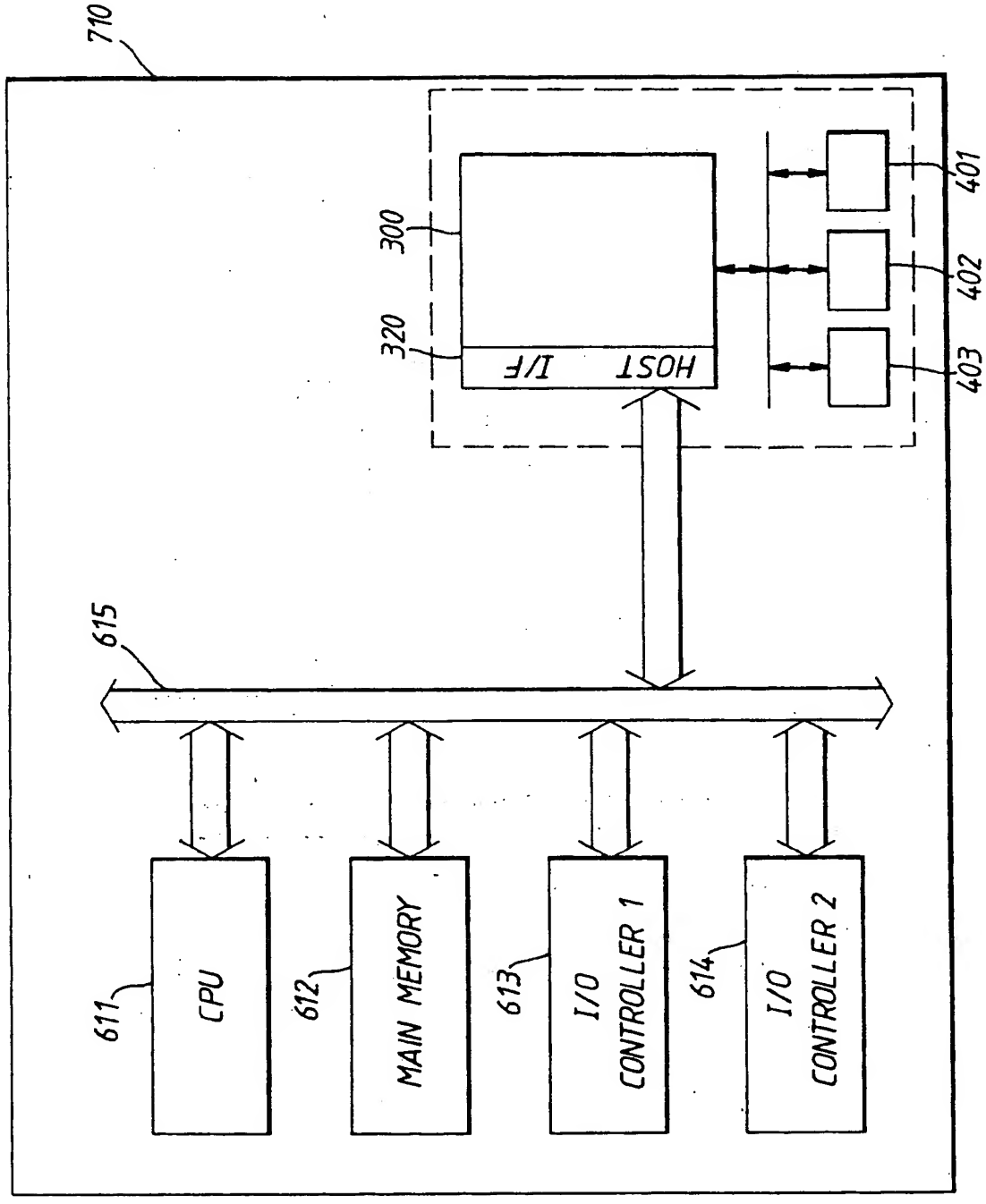


Fig.16

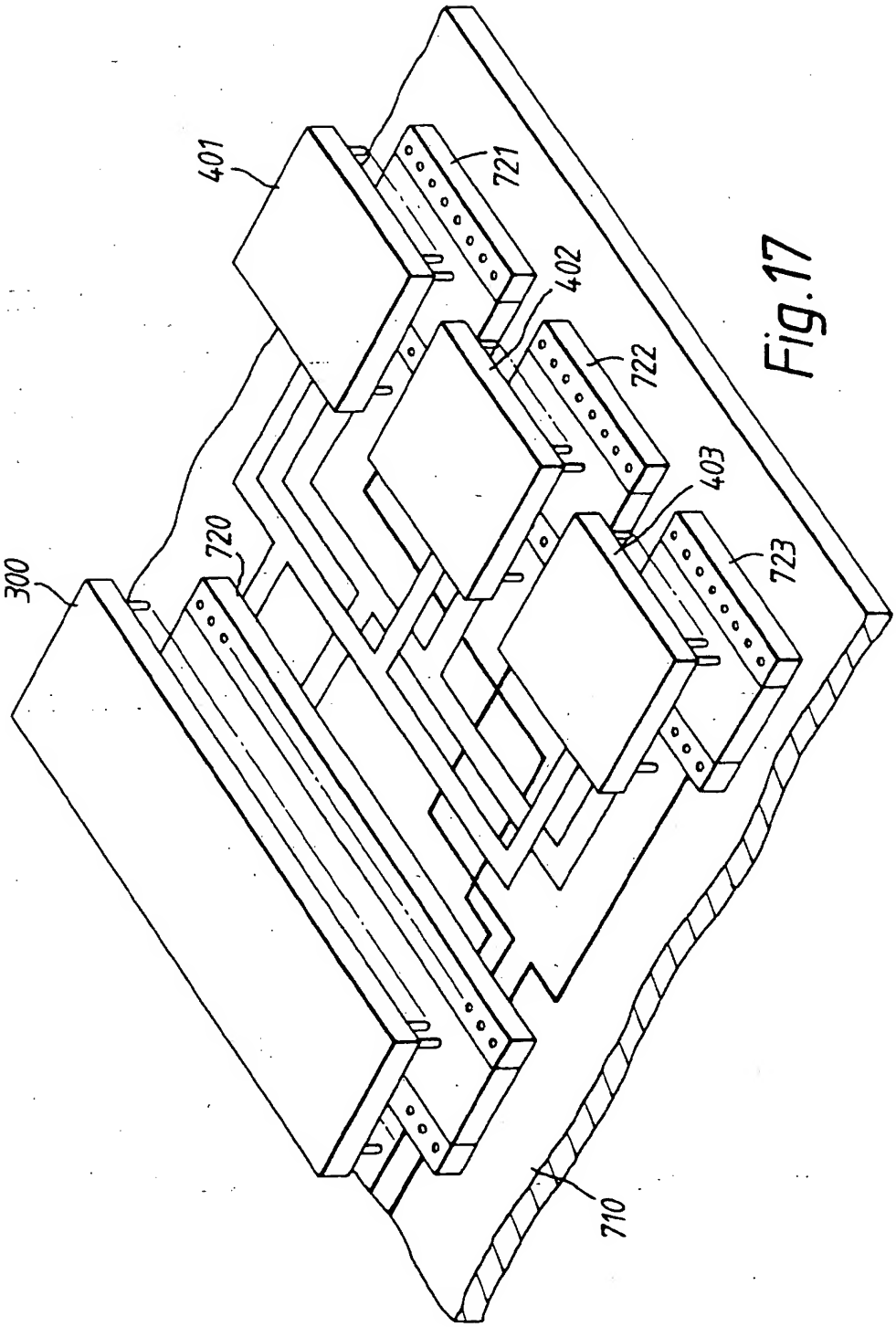


Fig.17

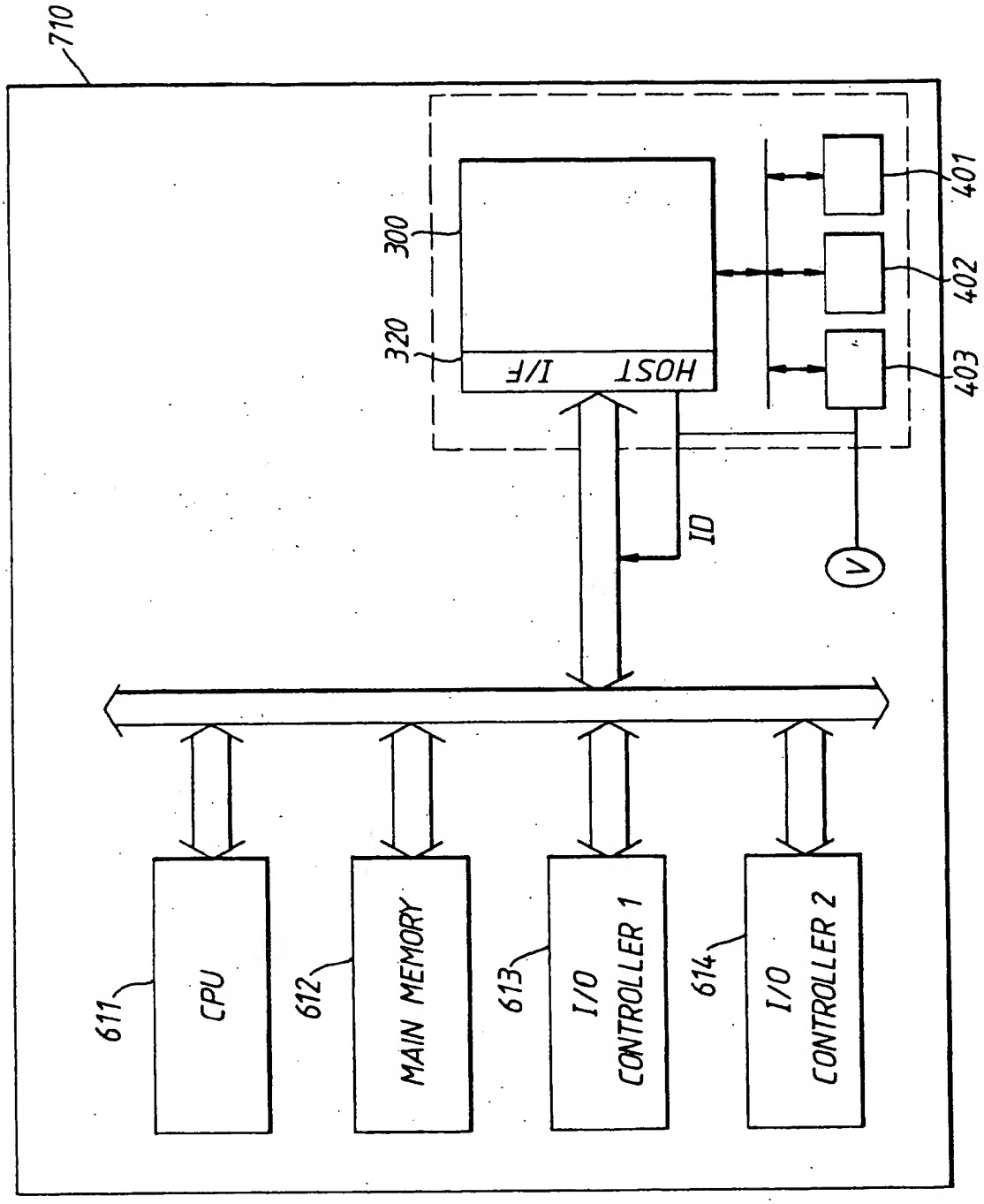


Fig.18

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 613 151 A3**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **94301320.1**

(51) Int. Cl.[5] : **G11C 16/06**, G06F 3/06

(22) Date of filing : **24.02.94**

(30) Priority : **26.02.93 JP 38112/93**
14.07.93 JP 173987/93
22.10.93 JP 264725/93

(43) Date of publication of application :
31.08.94 Bulletin 94/35

(84) Designated Contracting States :
DE FR GB

(88) Date of deferred publication of search report :
22.03.95 Bulletin 95/12

(71) Applicant : **KABUSHIKI KAISHA TOSHIBA**
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi Kanagawa-ken 210 (JP)

(72) Inventor : **Sukegawa, Hiroshi, c/o Intellectual Property Div.**
Toshiba Corp.,
1-1-1 Shibaura,
Minato-ku
Tokyo (JP)

(74) Representative : **BATCHELLOR, KIRK & CO.**
2 Pear Tree Court
Farringdon Road
London EC1R 0DS (GB)

(54) Semiconductor memory system including a flash EEPROM.

(57) A semiconductor memory system including A flash EEPROM comprises a first flash EEPROM (101, 102, 103) included in the first memory drive, a second flash EEPROM (104, 105, 106) included in the second memory drive, and an access controller (132) for controlling access to the first and second flash EEPROMs (101-106). The access controller (132) includes an address converting means for converting a logical address from a host system into a physical address, according to an address conversion table 150 which indicates correspondence between logical addresses and physical addresses of the first and second memory drives. The access controller (132) further includes memory accessing means, coupled to each of the first and second flash EEPROMs (101-106), for accessing a selected EEPROM according to the physical address from the address converting means.

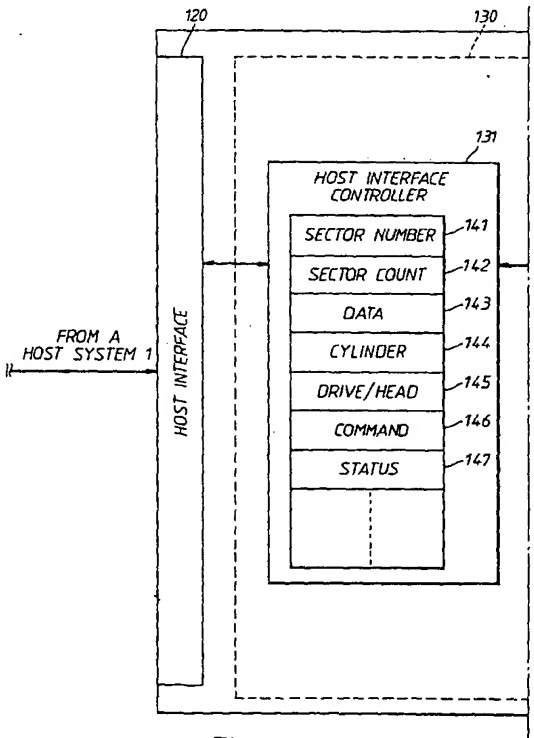


Fig.1a

EP 0 613 151 A3

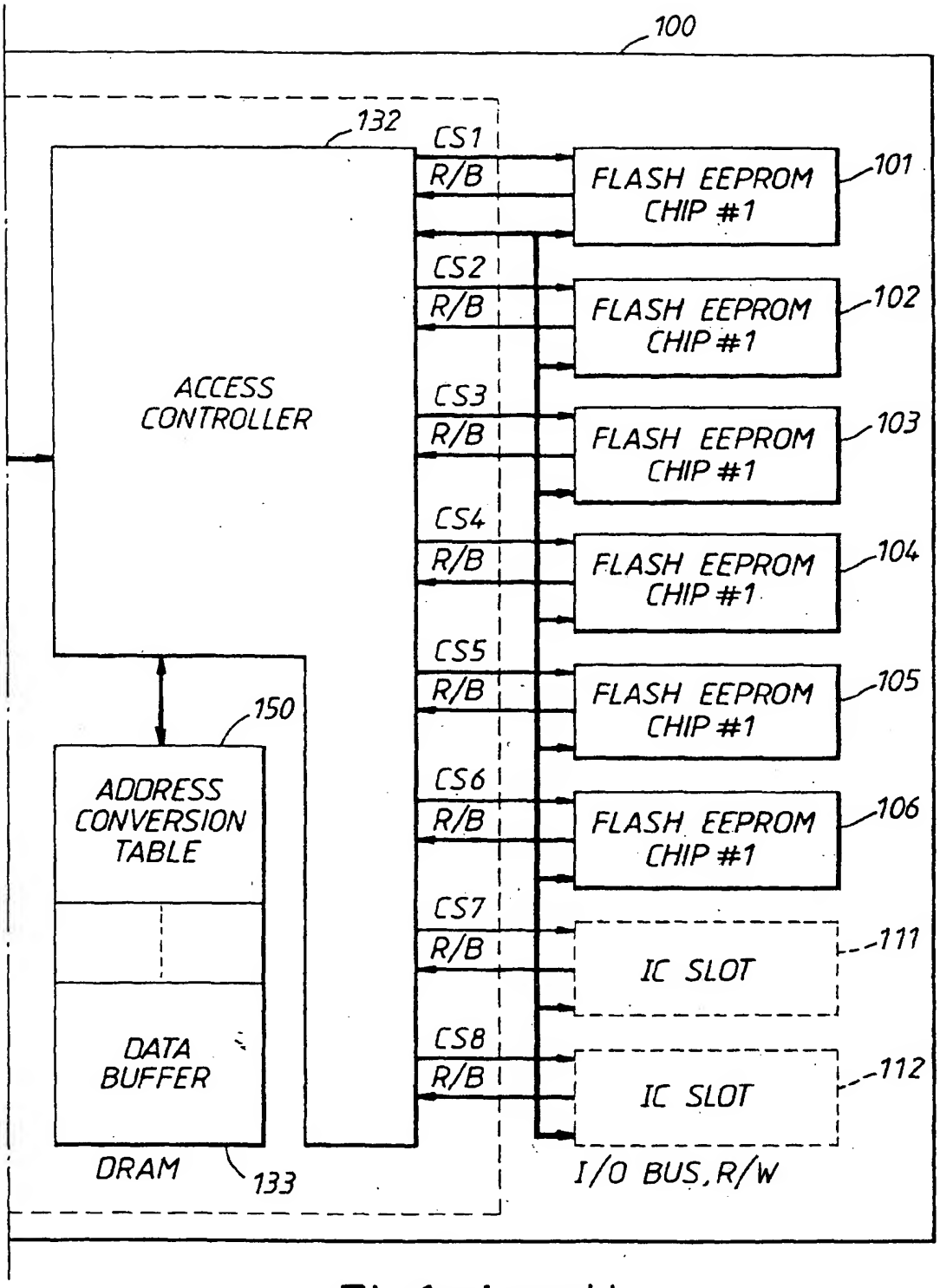


Fig.1a (cont)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 1320

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	PATENT ABSTRACTS OF JAPAN vol. 17, no. 82 (P-1489) 18 February 1993 & JP-A-04 283 825 (FUJITSU LTD) 8 October 1992 * abstract *	1,8,15, 16,18,20	G11C16/06 G06F3/06
A	EP-A-0 528 280 (TOSHIBA AVE) * column 5, line 29 - column 9, line 50; figures 2,3 *	1,3,8	
A	EP-A-0 477 503 (FUJI PHOTO FILM CO. LTD) * column 5, line 4 - column 7, line 36; figures 1,2 *	15,16	
A	IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE., vol.36, 24 February 1993, NEW YORK US pages 52 - 53 WELLS ET AL 'Flash solid-state drive with 6MB/s reas/write channel and data compression'		

TECHNICAL FIELDS SEARCHED (Int.Cl.5)
G11C
G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13 January 1995	Cummings, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

FIG 1

(PRIOR ART)

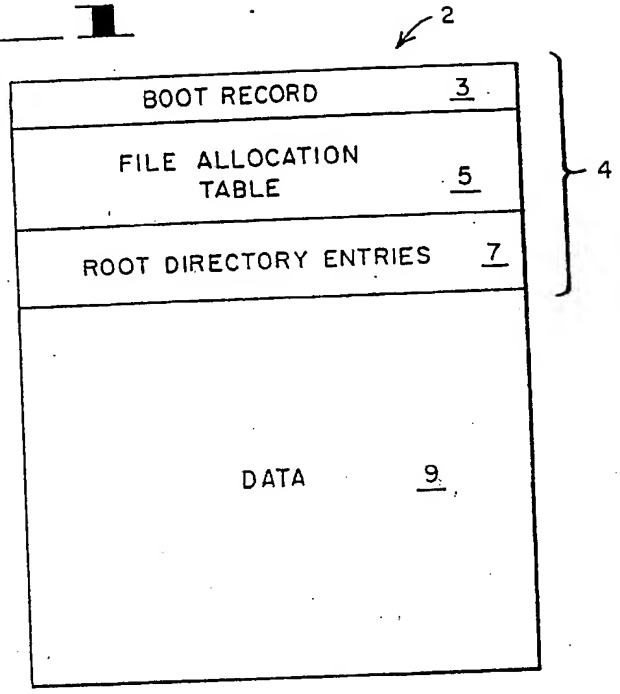


FIG 2

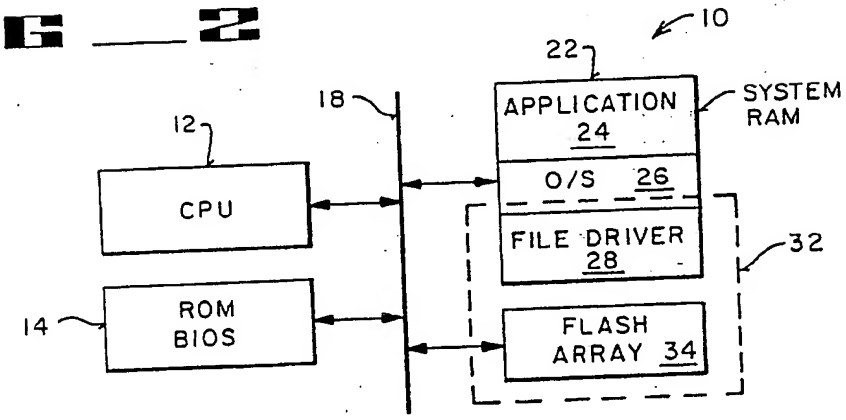


FIG 3

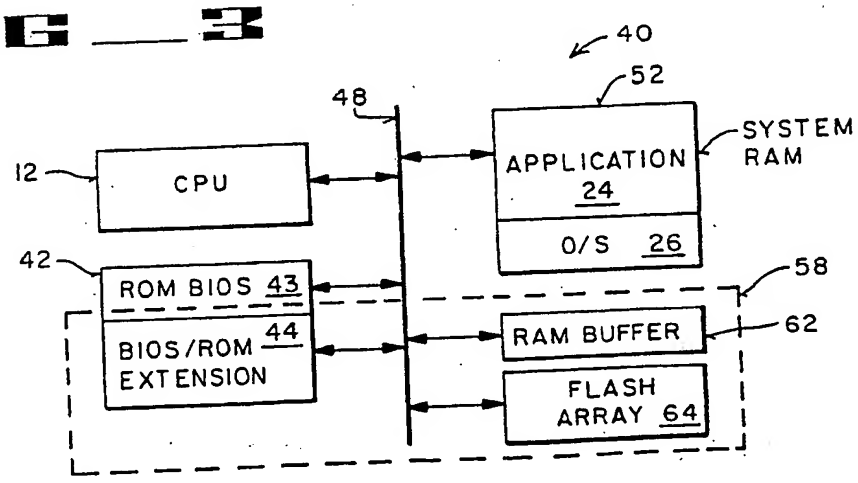


FIG 4

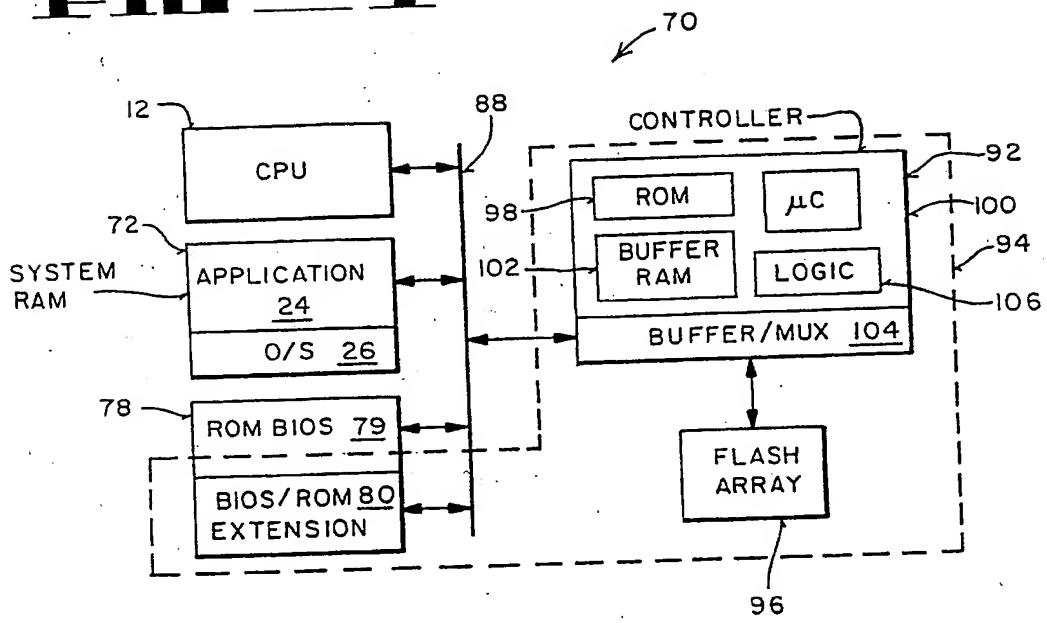


FIG 5

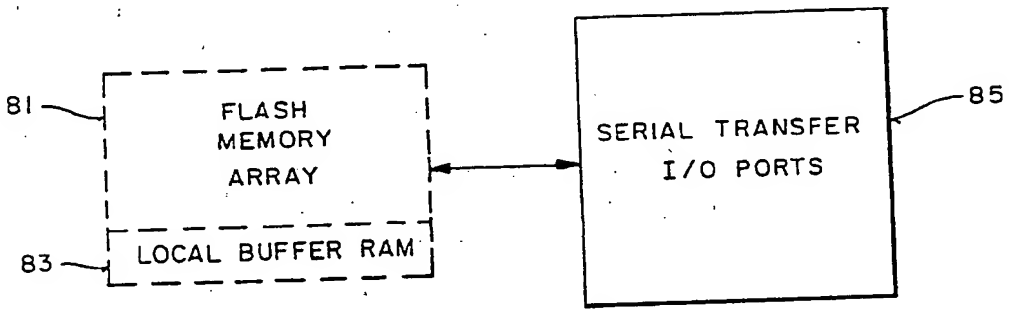


FIG 6

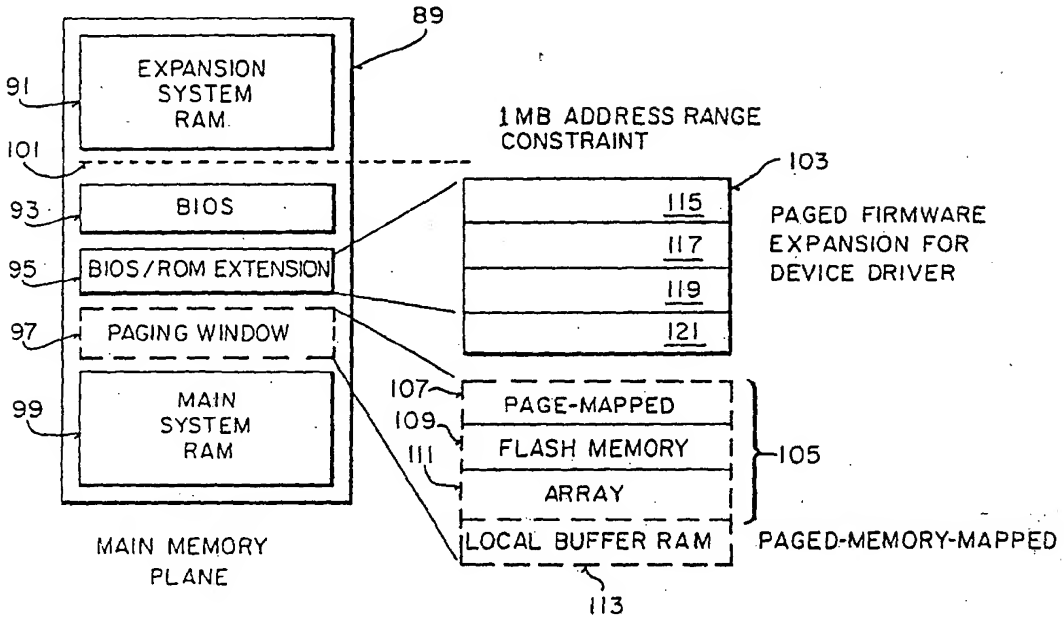
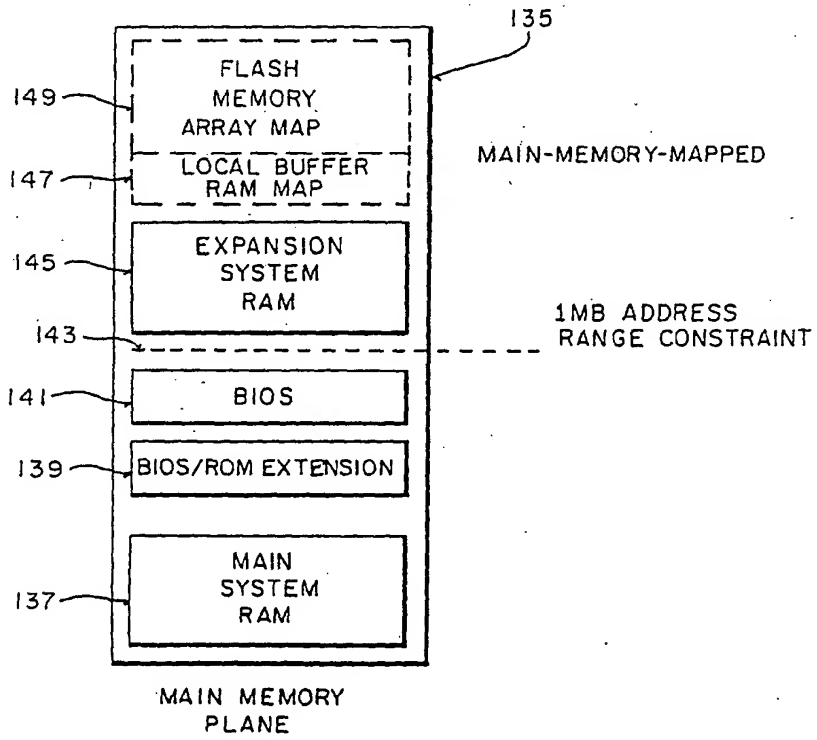

89
91
EXPANSION SYSTEM RAM
101
1MB ADDRESS RANGE CONSTRAINT
103
93
BIOS
115
117
119
121
PAGED FIRMWARE EXPANSION FOR DEVICE DRIVER
95
BIOS/ROM EXTENSION
97
PAGING WINDOW
99
MAIN SYSTEM RAM
107
109
111
PAGE-MAPPED
FLASH MEMORY
ARRAY
105
LOCAL BUFFER RAM
PAGED-MEMORY-MAPPED
113
MAIN MEMORY PLANE

FIG 7


135
149
FLASH MEMORY ARRAY MAP
147
LOCAL BUFFER RAM MAP
MAIN-MEMORY-MAPPED
145
EXPANSION SYSTEM RAM
143
1MB ADDRESS RANGE CONSTRAINT
141
BIOS
139
BIOS/ROM EXTENSION
137
MAIN SYSTEM RAM
MAIN MEMORY PLANE

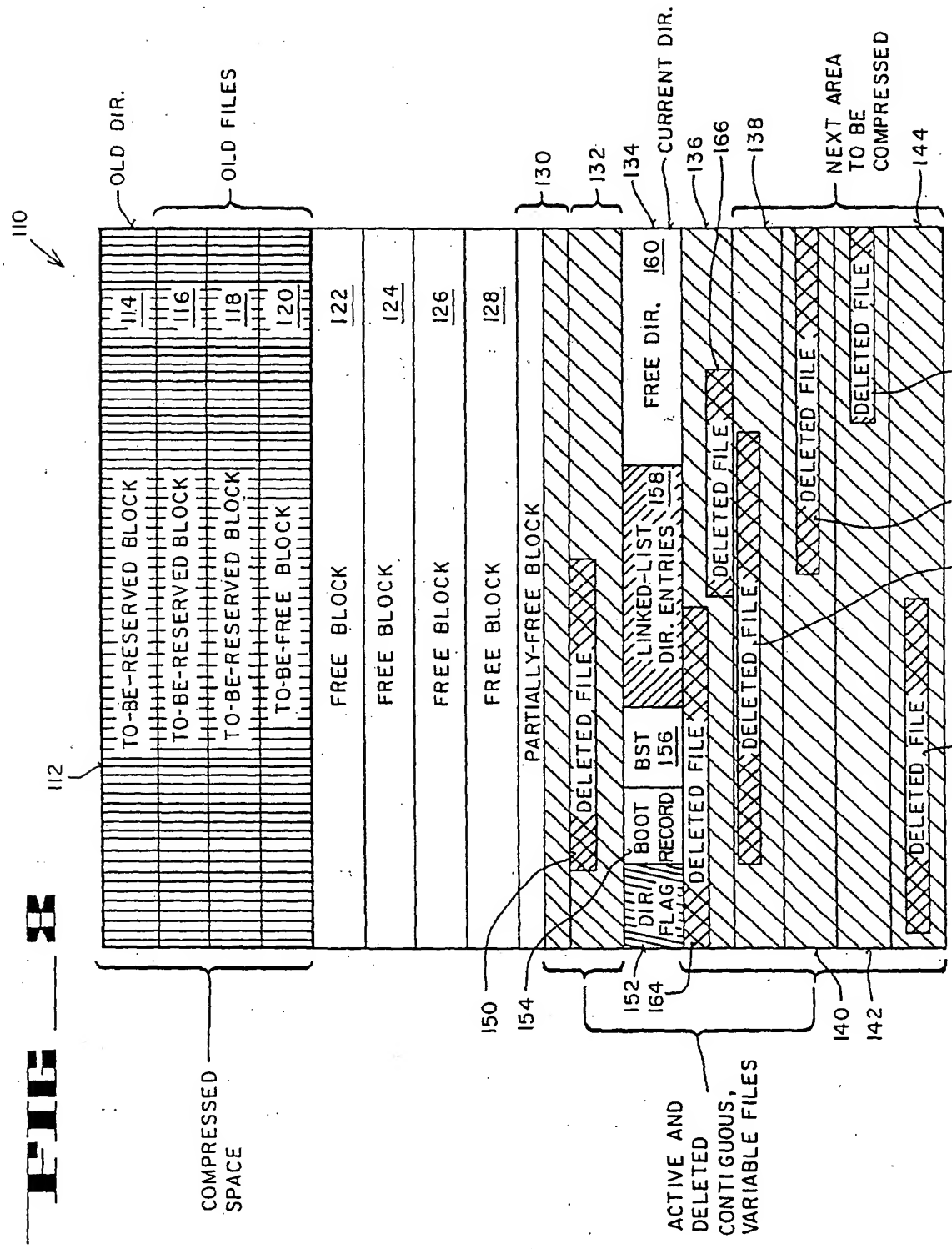


FIG — 8

FIG 9

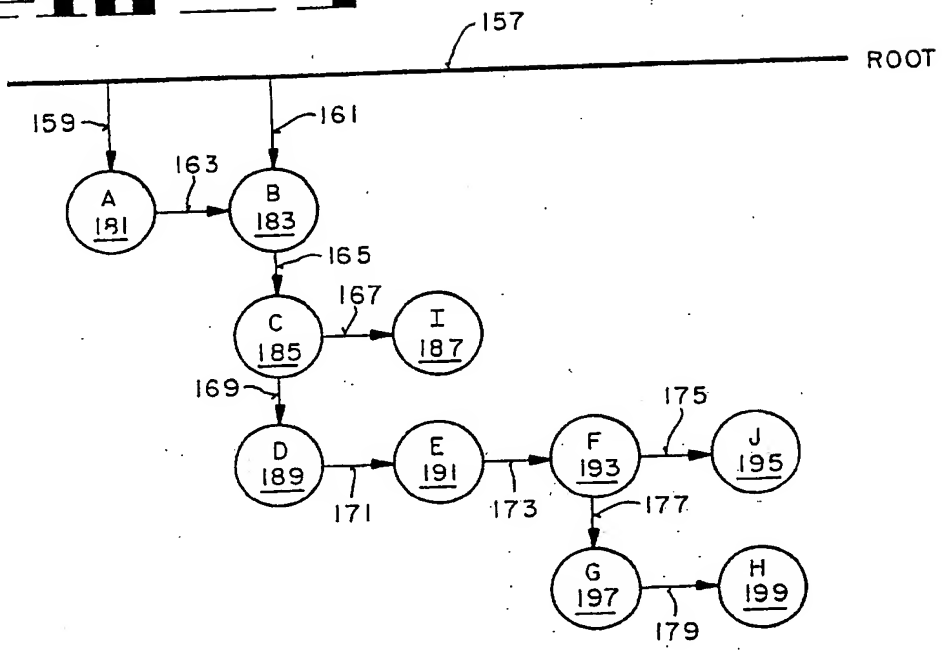
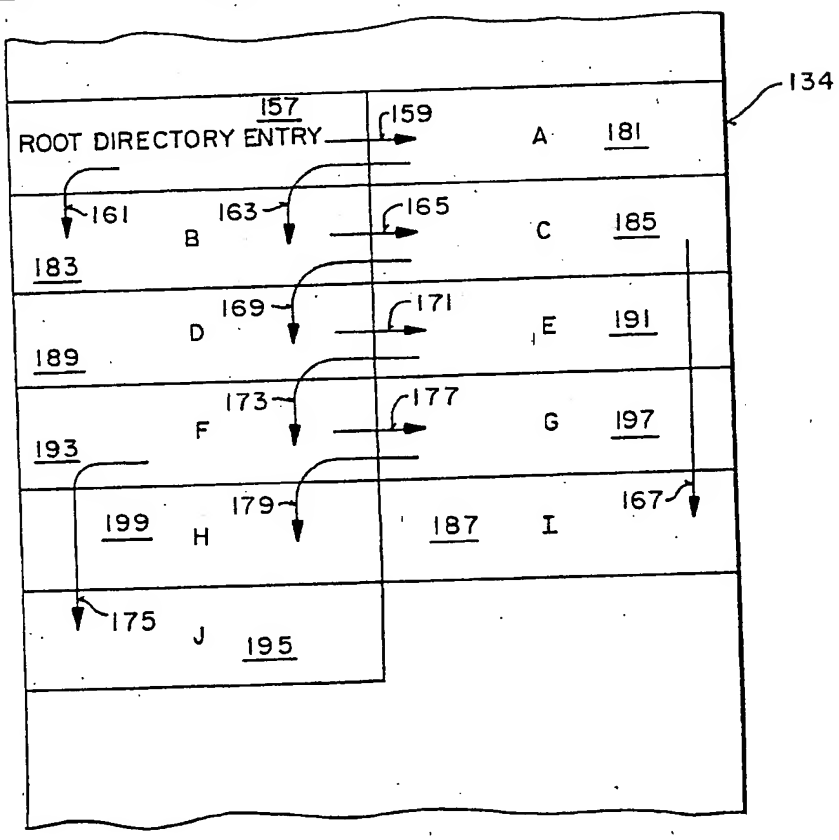

157
ROOT
159
161
163
A
181
B
183
165
C
185
167
I
187
169
D
189
E
191
F
193
175
J
195
171
173
177
G
197
H
199
179

FIG 10


134
157
ROOT DIRECTORY ENTRY
159
A
181
161
163
165
B
183
C
185
169
171
D
189
E
191
173
177
F
193
G
197
167
199
H
179
187
I
175
J
195

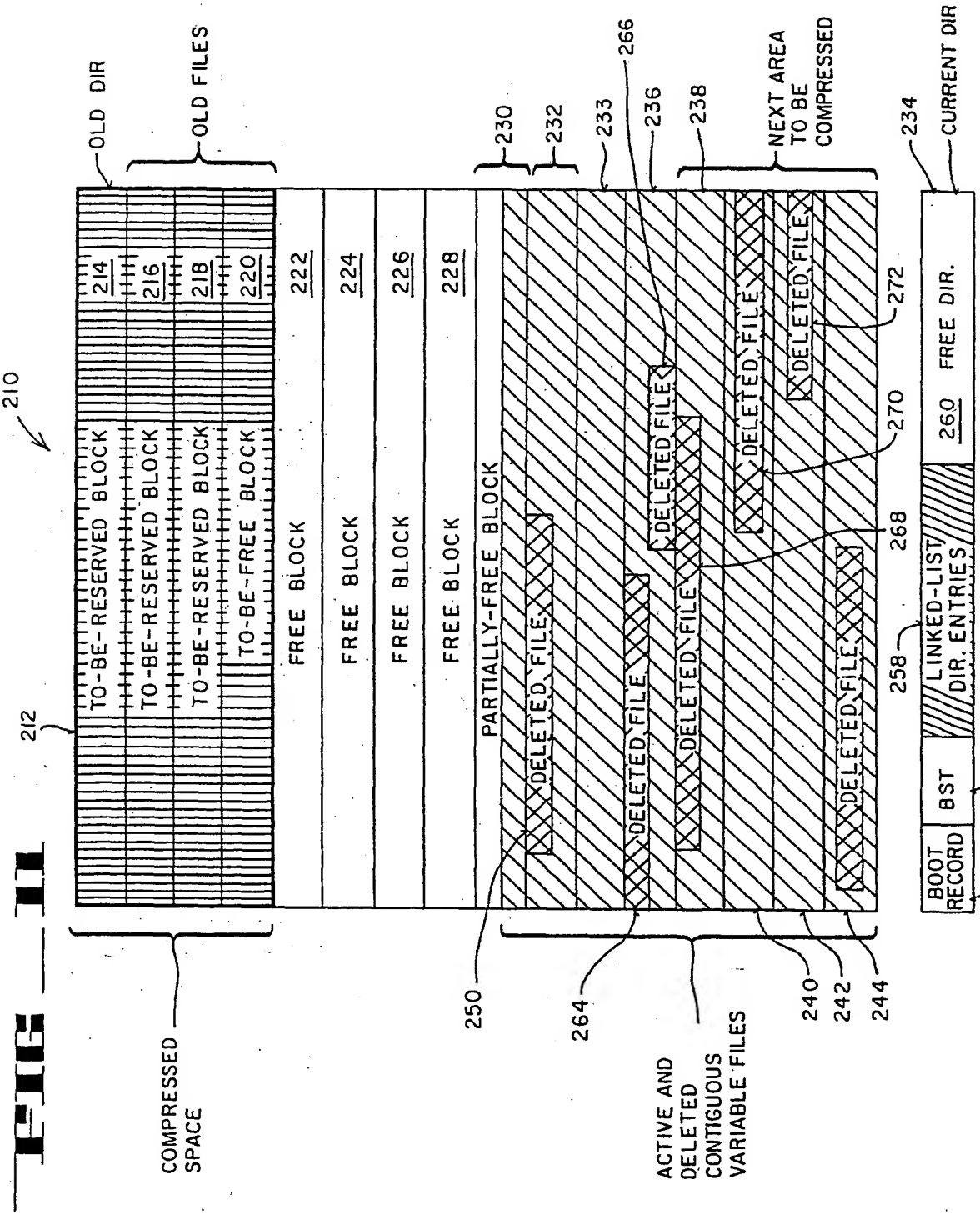
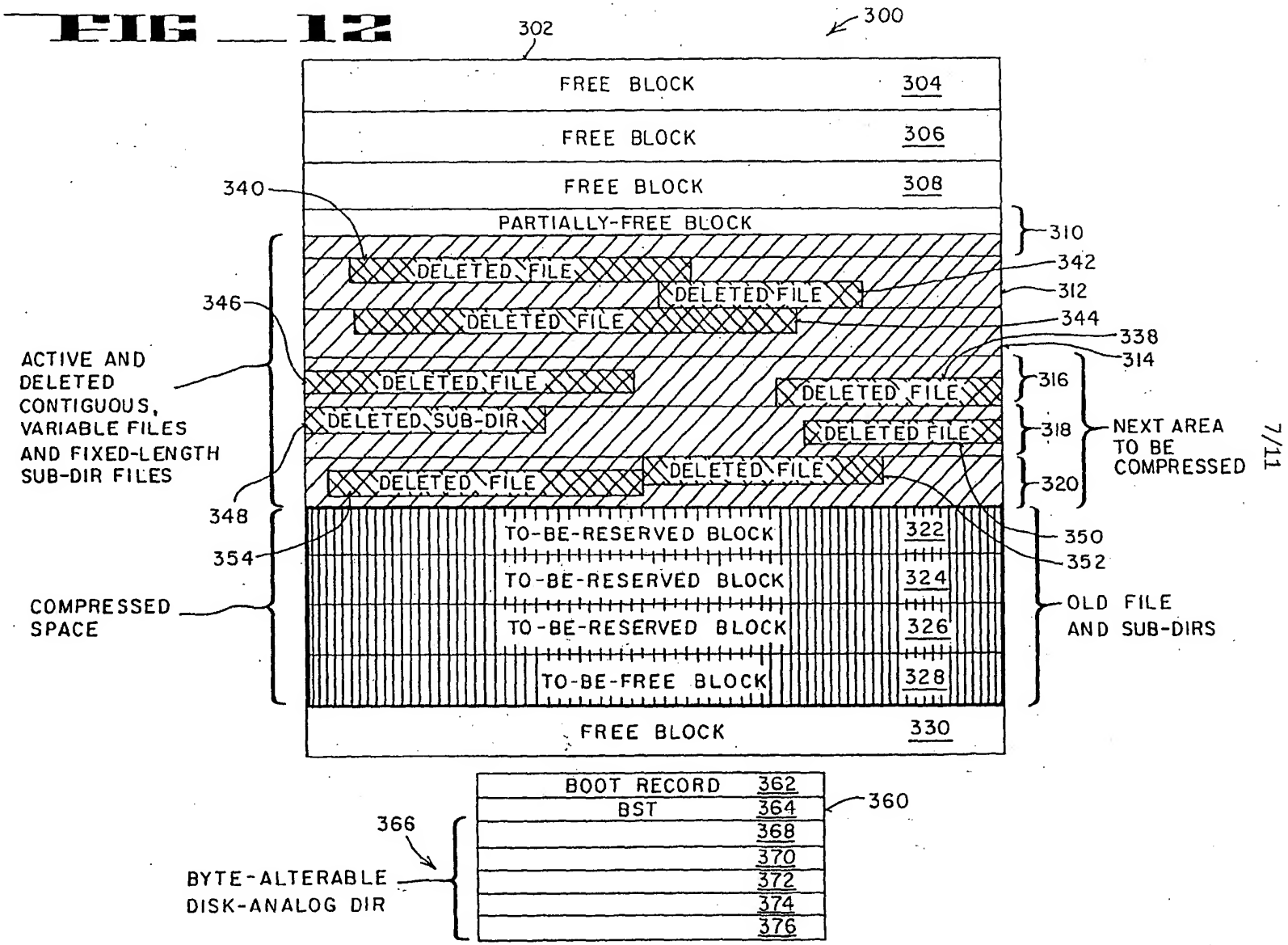
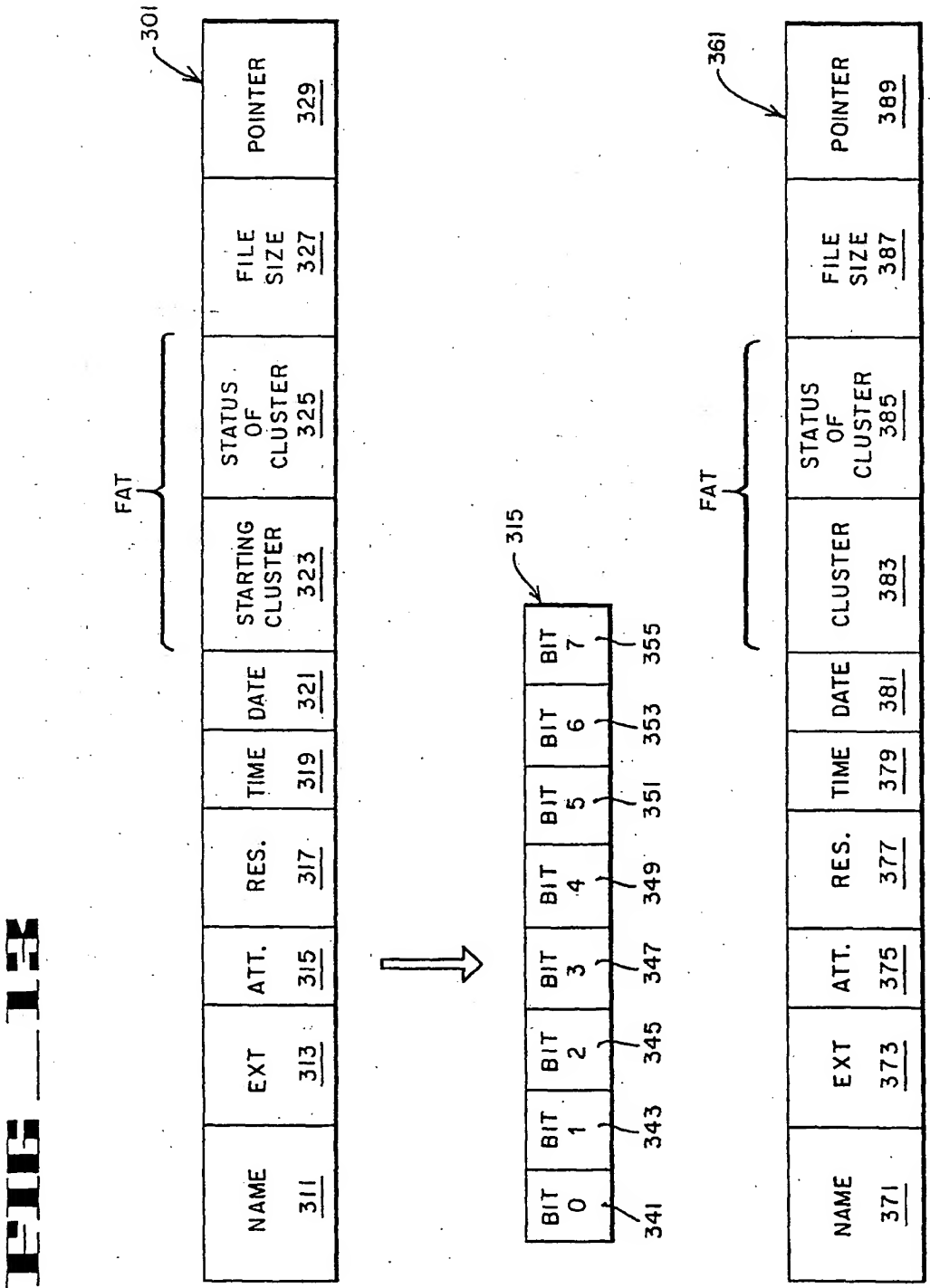


FIG 12


300
302
FREE BLOCK 304
FREE BLOCK 306
FREE BLOCK 308
PARTIALLY-FREE BLOCK
310
340
342
312
344
338
314
346
DELETED FILE
DELETED FILE
DELETED FILE
DELETED FILE
DELETED FILE
DELETED FILE
DELETED SUB-DIR
DELETED FILE
DELETED FILE
316
318
320
NEXT AREA TO BE COMPRESSED
ACTIVE AND DELETED CONTIGUOUS, VARIABLE FILES AND FIXED-LENGTH SUB-DIR FILES
348
354
TO-BE-RESERVED BLOCK 322
TO-BE-RESERVED BLOCK 324
TO-BE-RESERVED BLOCK 326
TO-BE-FREE BLOCK 328
350
352
COMPRESSED SPACE
OLD FILE AND SUB-DIRS
FREE BLOCK 330
BOOT RECORD 362
BST 364
360
366
368
370
372
374
376
BYTE-ALTERABLE DISK-ANALOG DIR

7/11

FIG. 15



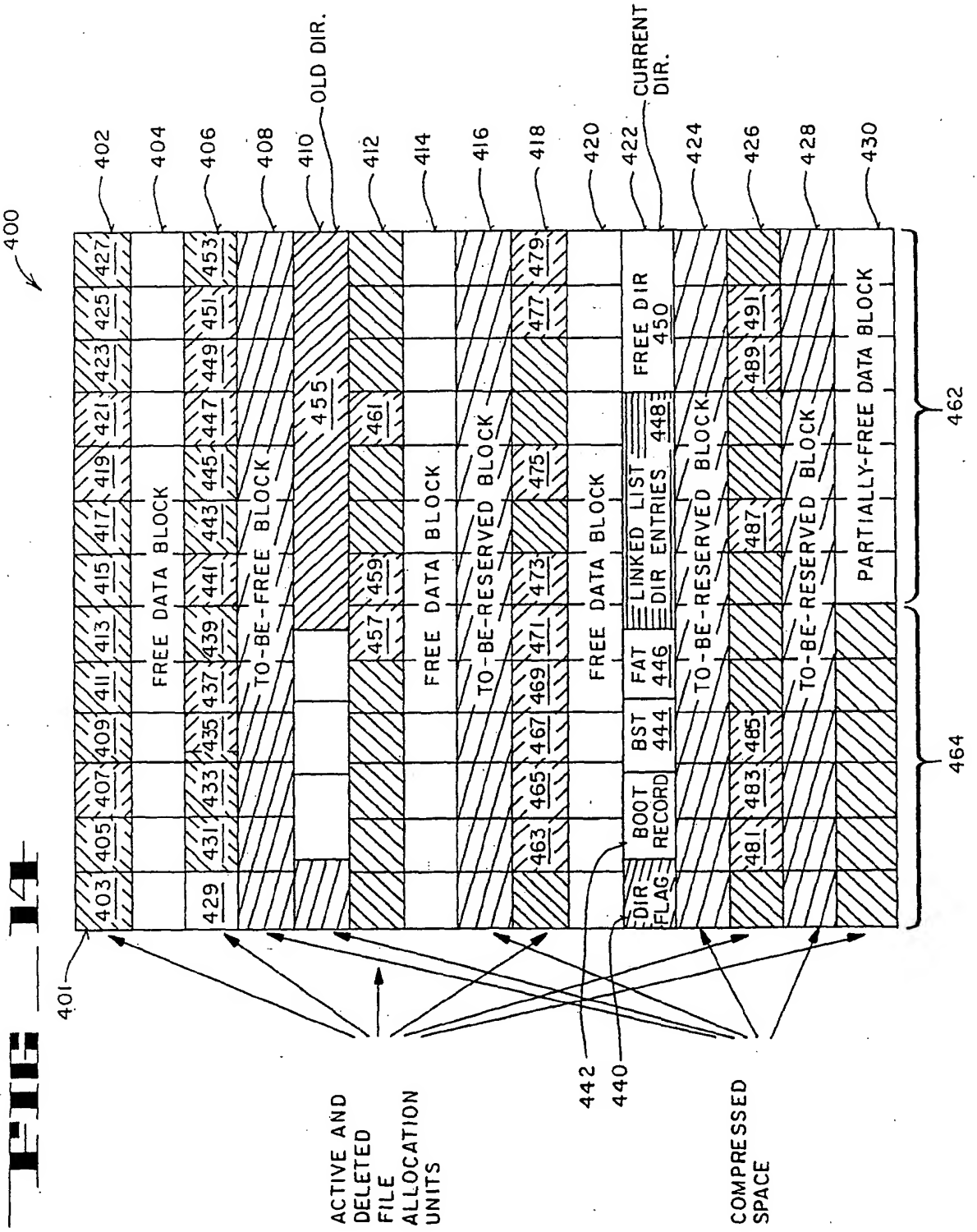


FIG — 14